





IPC/JPCA-2315

Design Guide for High Density Interconnects (HDI) and Microvias

IPC/JPCA-2315

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A joint standard developed by IPC and JPCA

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Developed by the High Density Interconnect (HDI) Design Subcommittee (D-41) of the High Density Interconnect (HDI) Committee (D-40) of IPC and the Build-Up PWB Committee of the Japan Printed Circuit Association (JPCA)

Users of this standard are encouraged to participate in the development of future revisions.

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Acknowledgment

Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the High Density Interconnect (HDI) Design Subcommittee (D-41) of the High Density Interconnect (HDI) Committee (D-40) and the JPCA Build-Up PWB Committee are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC and JPCA extend their gratitude.

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Design Guide for High Density Interconnects (HDI) and Microvias

1 SCOPE

This document describes various via formations, materials, and design guidelines used in high density interconnects (HDI) and microvias. Microvias are processed/plated holes ≤0.15 mm in diameter.

1.1 Introduction This document is intended to educate the user on the formation of microvias and the selection of wiring density, design rules, interconnects, and materials. It is intended to provide design guidelines for PWBs utilizing microvia technologies.

1.2 General This document is intended to help in the selection of the preferred advanced technology for electronic packaging. The microvia PWBs are commonly referred to as build-up (BU) or sequential build-up (SBU) PWBs. These design rules apply to the BU and SBU interconnects using materials defined in IPC/JPCA-4104. The characteristics of these materials are found in Section 5.

1.3 HDI Design Selection Guideline This guideline provides an easy to follow tutorial on the selection of HDI and microvia design rules and structures. This document brings the user through various considerations to be addressed when designing an HDI PWB, including:

- Design examples and processes
- Selection of materials
- General descriptions
- Various microvia technologies (i.e., variable depth vias and stacked vias)

1.4 Design Figures Figure 1-1 is a color key to be used with all of the figures in this document. The key shows the color next to the material it represents.

2 APPLICABLE DOCUMENTS[1]

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC/JPCA-4104 Specification for High Density Interconnect (HDI) and Microvia Materials

IPC/JPCA-6801 Terms and Definitions, Test Methods, and Design Examples for Build-Up/High Density Interconnect (HDI) Printed Wiring Boards

Build-Up Material
Prepreg/Adhesive
Soldermask
Core Material
Flex
Conductive Paste
Bumper Conductive
Conductive Ink/Hole Fill
Vendor Copper
Plating
Anisotropic Conductive Material
IPC-2315-1-01

Figure 1-1 Color Key

3 TERMS AND DEFINITIONS

Terms and definitions shall be in accordance with IPC-T-50, IPC/JPCA-6801, and IPC/JPCA-4104.

3.1.1 Capture Land Land where the microvia starts; varies in shape and size based on use (i.e., component mounting, via entrance, and conductor).

3.1.2 Target Land Land on which a microvia ends and makes a connection.

3.1.3 Stacked Vias A via formed by stacking one or more microvias on a PTH that provides an interlayer connection between three or more conductive layers.

3.1.4 Stacked Microvia A microvia formed by stacking one or more microvias on a microvia that provides an interlayer connection between three or more conductive layers.

4 MICROVIAS

Microvias, which began in the late 1980s, are the central characteristic of HDI PWBs (see Figure 4-1). The original methods for developing microvias were by plasma desmear

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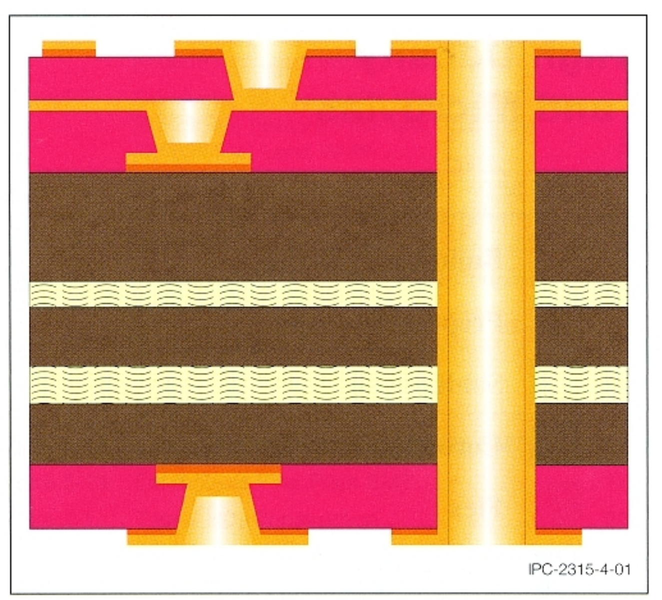


Figure 4-1 Cross Section of a General HDI with Microvias

and photodeveloping. As explained in 4.1, there are now five general ways of producing microvias.

4.1 Via Formation There are five general processes for microvia formation:

- Laser drilling
- Wet/dry etching
- Photo imaging
- Conductive ink-formed vias
- Mechanical formation

Although this section is not intended to describe all microvia formation methods, microvias can be grouped into the following three methodologies:

- Create hole then make conductive.
- Create conductive via then add dielectric.
- Create conductive via and dielectric simultaneously.

The microvia can be any shape, including straight wall, positive or negative taper, or cup. All drawings in this guideline are the artist's rendering; the hole wall shape doesn't represent the actual finished product. The techniques shown in Figure 4-2 and Figure 4-3 could be used for producing microvias.

All of these technologies require approximately the same HDI design rules and have four to eight times the wiring density of conventional, drilled PTHs.

4.1.1 Laser Ablated Vias Laser ablation is a single or multiple via generation technology that replaces mechanical drilling with lasers. Laser ablation differs from mechanical drilling in that the focused beam used to create the vias can produce smaller holes. These lasers are generally categorized by their wavelength of light. They can be used to create both blind vias and through holes. The process normally occurs after multilayer lamination and is

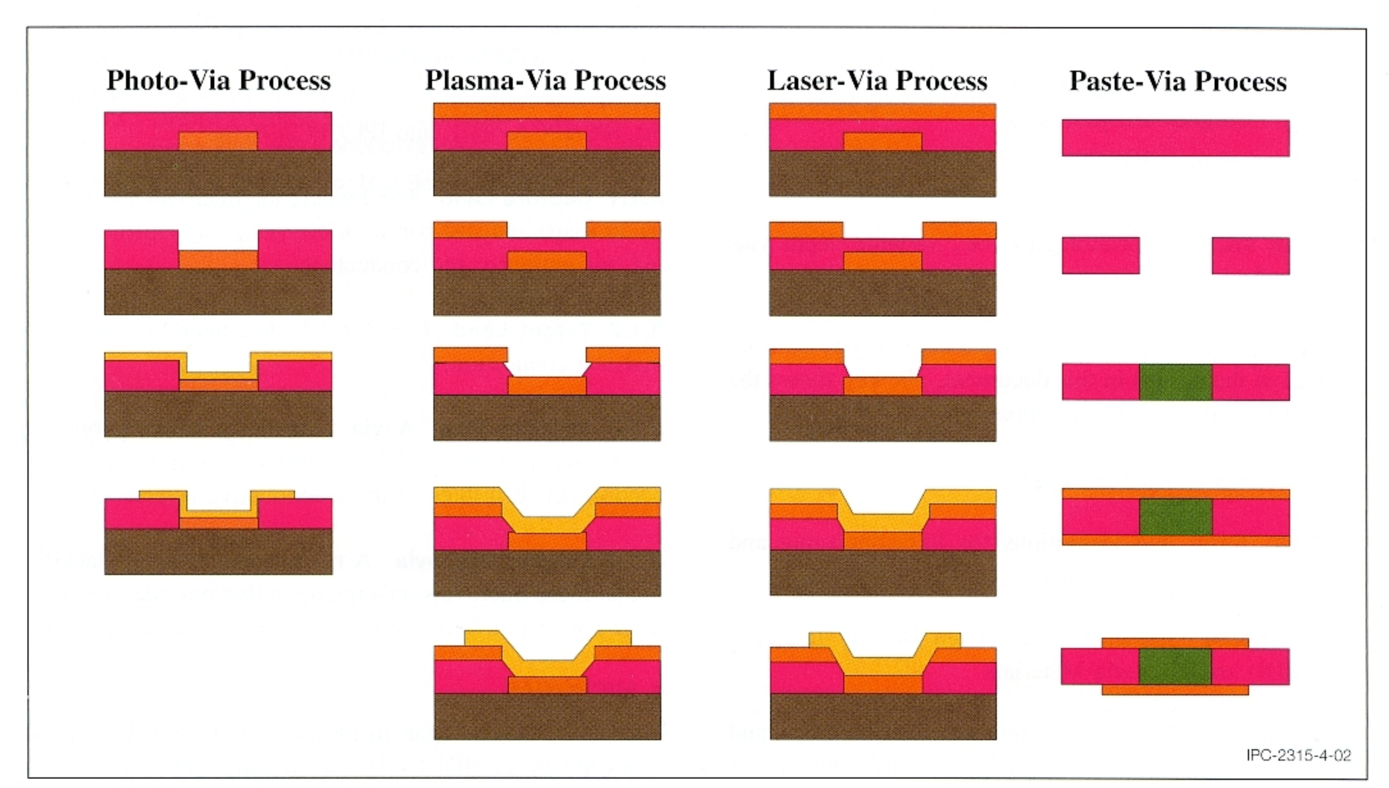


Figure 4-2 Microvia Manufacturing Processes

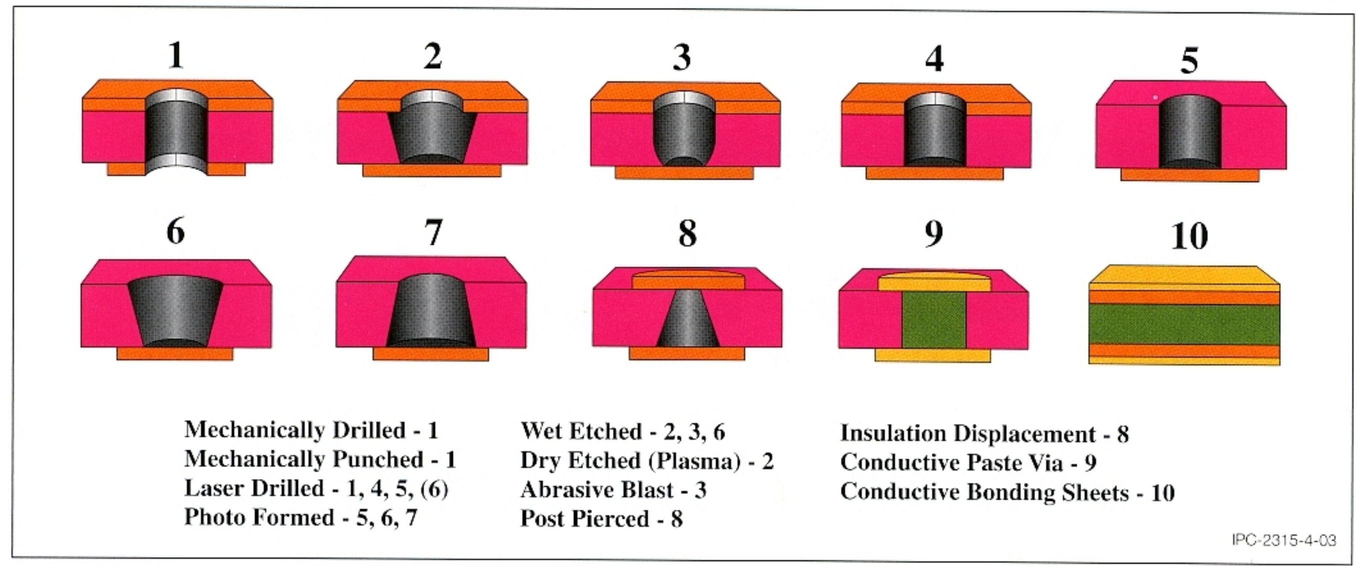


Figure 4-3 Cross-Sectional Views of Methods to Make HDI with Microvias

compatible with most materials. Laser-based microvia technologies are capable of smaller features and use standard plating technology. In the majority of cases, laser ablation produces blind or through vias one at a time, but there are processes for generating multiple laser vias simultaneously.

The four technologies represented in Figure 4-4 are just a few of those published in literature and being developed as of publication of this document. These are the oldest of the HDI technologies, employing lasers to produce microvias.

4.1.2 Wet/Dry Etched Vias Microvias can be formed by various etching techniques. The most common etching technique is a microwave gas plasma, dry etching process. Wet etching by hot KOH has been used historically for polyimide films. Because of the chemical effects, these formation techniques are isotropic, that is they etch in all directions while they etch down. Alternate processes show that anisotropic etching can give more perpendicular sides. These formation techniques are mass via generation in that they form all vias at the same time without regard to number or diameter.

Figure 4-5 gives four examples of technologies that are developed through wet and dry etching and mechanical formation.

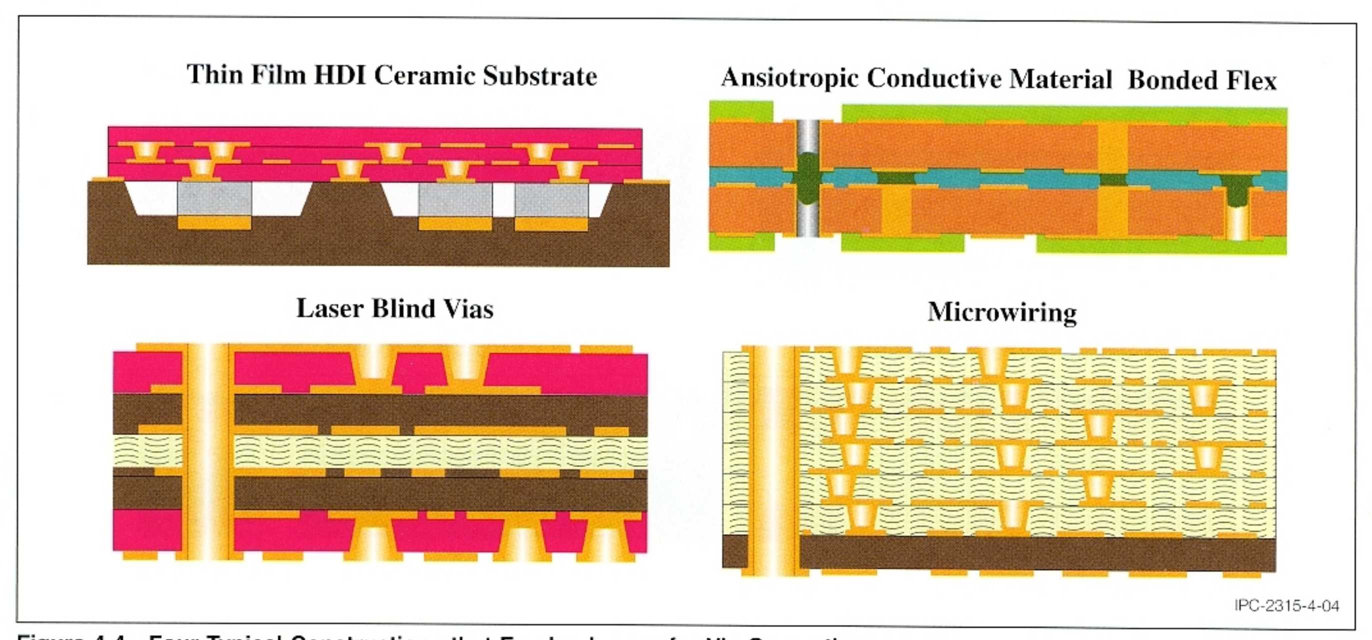


Figure 4-4 Four Typical Constructions that Employ Lasers for Via Generation

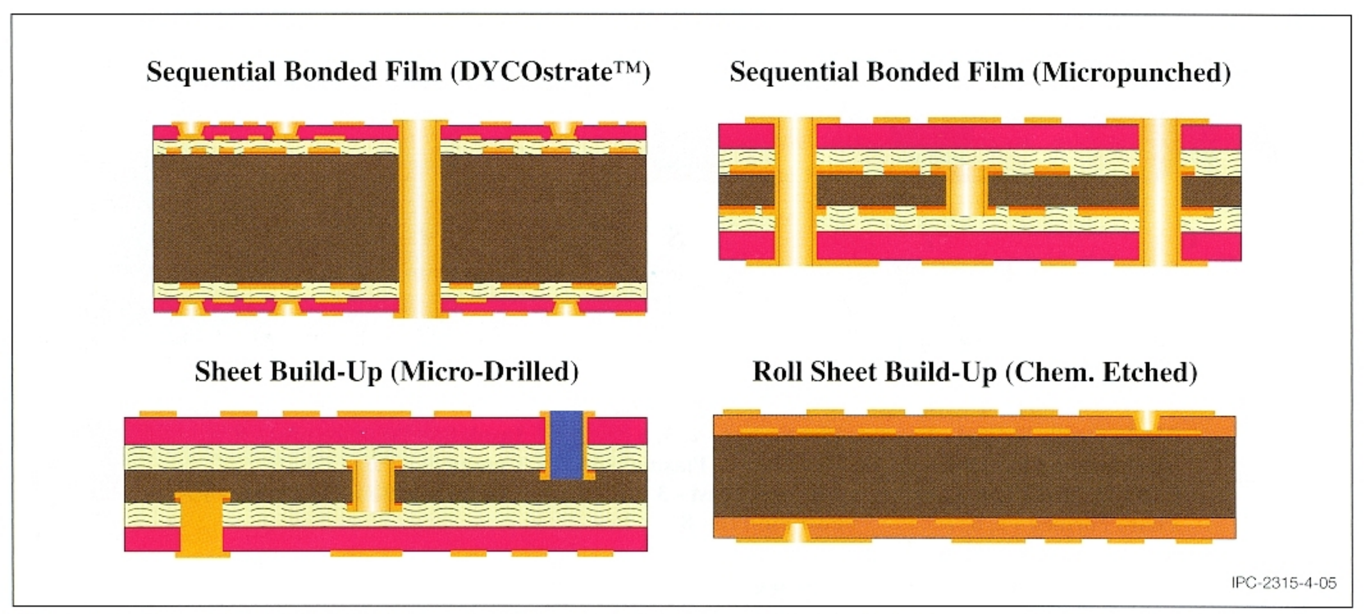


Figure 4-5 Four Typical Constructions Utilizing Etched or Mechanically Formed Vias

4.1.3 Photodielectric Vias Figure 4-6 displays a dielectric layer coated over a core substrate with PTHs and/or plugged holes. Microvias are formed by photoimaging. A layer of dielectric is coated over the base substrate. The microvias or circuit paths are imaged, developed, cured, and subsequently metallized to allow for patterning.

First used in 1988, the photoimageable dielectric was a modified solder mask. Today, modern photoimageable dielectrics (PID) are optimized as a dielectric in liquid or dry film and can be positive or negative acting. This is also a mass via generation technique, forming all vias in a single operation.

4.1.4 Conductive Inks/Insulation Displacement Figure 4-7 shows a dielectric layer with microvias formed by photoimaging, laser, or insulation displacement. A conductive paste is used to fill the microvias and act as the conductive path between layers. Surface metallization may be accomplished by either laminating copper foil onto the dielectric surface or by chemical deposition.

4.1.5 Process Flow for Via Formation Figure 4-8 is a process flow diagram of the manufacturing processes that employ PIDs, UV, or CO_2 laser ablation, and plasma etching to form microvias.

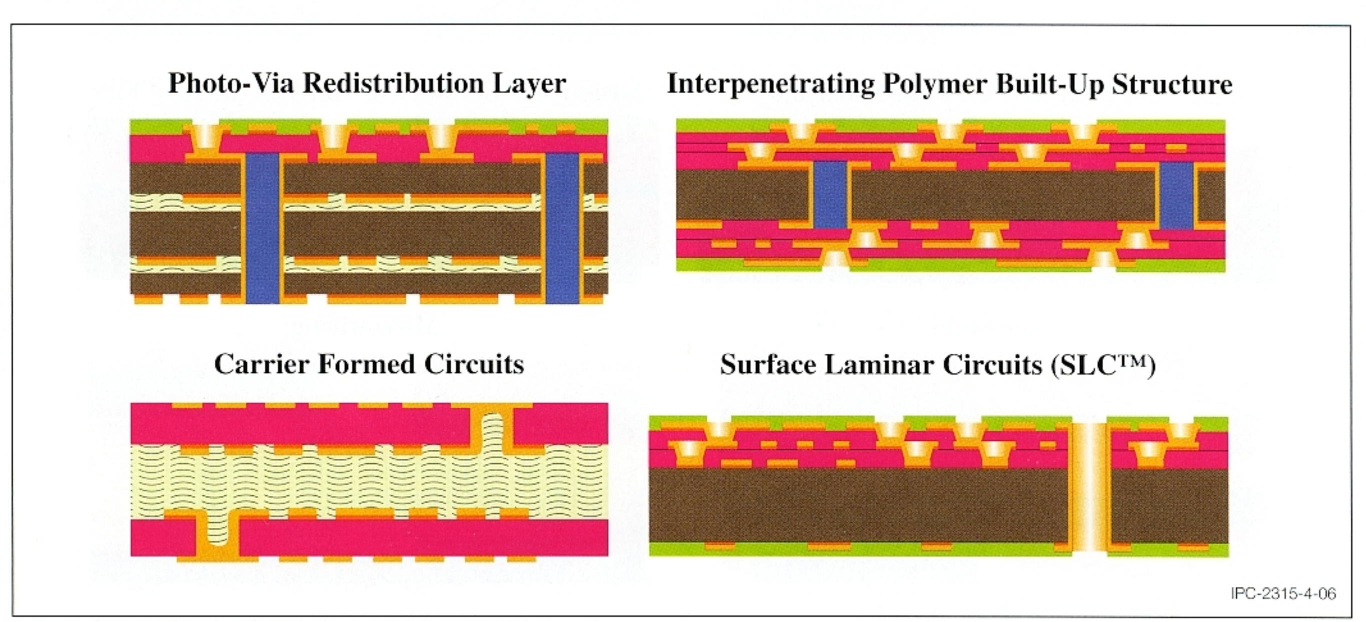


Figure 4-6 Four Commercially Produced PID Boards

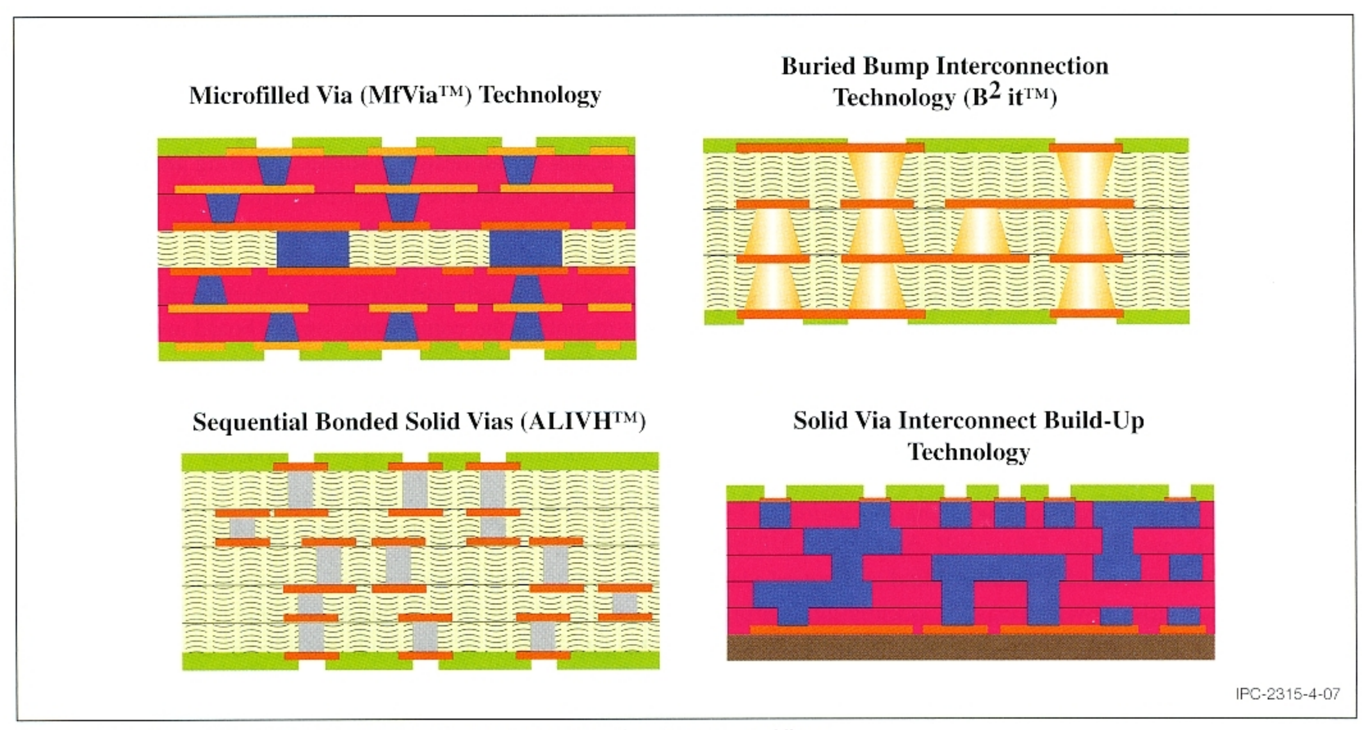


Figure 4-7 Four New HDI Boards that Employ Conductive Pastes as Vias

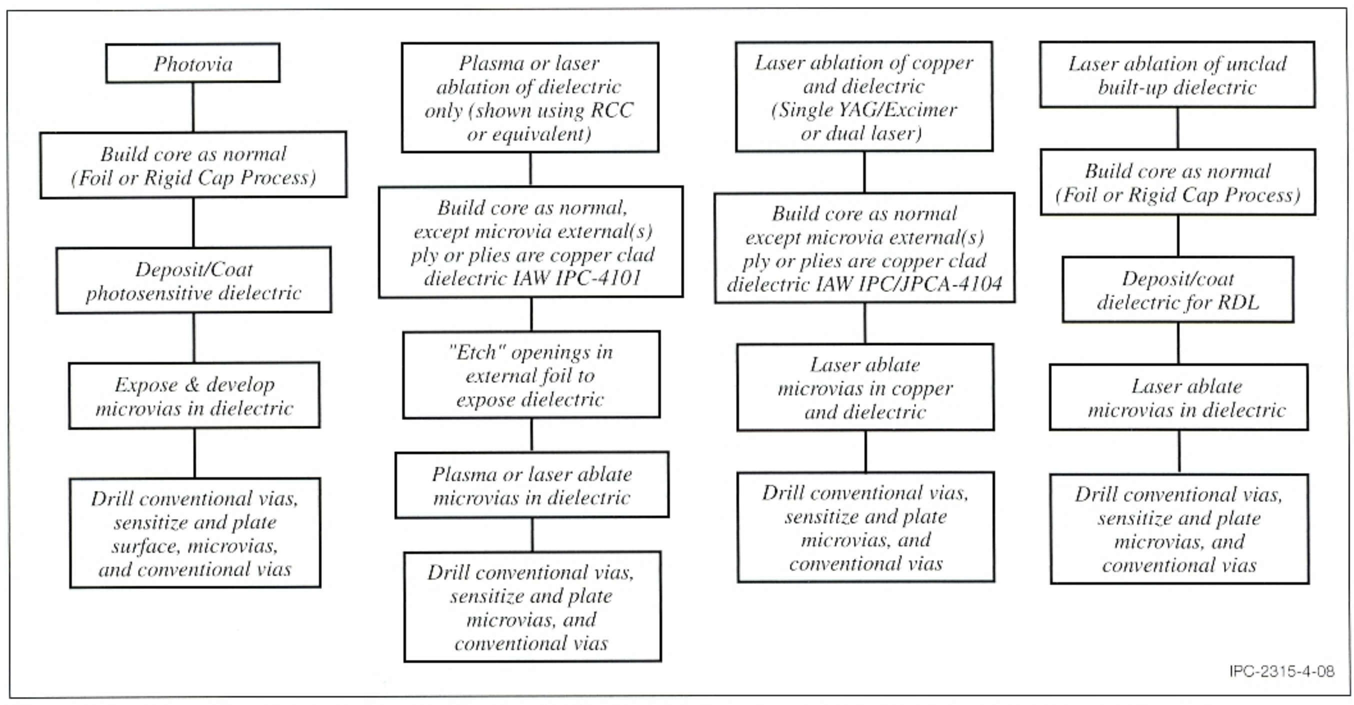


Figure 4-8 Summary of the Manufacturing Processes for PIDs, Laser, and Plasma Methods of Via Generation

5 DENSITY EVALUATION

A wide variety of materials and processes have been used to create substrates for electronics over the last half century, from traditional printed circuits made from resins (i.e., epoxy), reinforcements (i.e., glass cloth or paper), and metal foil (i.e., copper), to ceramics metallized by various thin and thick film techniques. However, they all share a common attribute; they must route signals through conductors. There are also limits to how much routing each can accommodate. The factors that define the limits of their wire routing ability as a substrate are:

- Pitch/distance between vias or holes in the substrate
- Number of wires that can be routed between those vias
- Number of signal layers required

In addition, the methods of producing blind and buried vias can facilitate routing by selectively occupying routing channels. Vias that are routed completely through the printed board preclude any use of that space for routing on all conductor layers.

These factors can be combined to create an equation that defines the wire routing ability of a technology. In the past, most components had terminations along the periphery on two or more sides. However area array components are more space conservative and allow coarser I/O pitches to be used (see Figure 5-1). See 5.4, which shows that very high I/O devices will require very dense substrate routing in order to interconnect the devices.

5.1 Routability Prediction Methods

5.1.1 Substrate Wiring Capacity Analysis After the approved schematic/logic diagrams, parts lists, and end-product and testing requirements are provided, and before the actual layout design is started, a wiring analysis-density evaluation should be conducted. This is based on all the parts contained in the parts list but excludes the interconnection conductors. The area usage is calculated using the largest space each part occupies, including the land pattern for mounting the components on the board and "keep out" areas for "step downs" of solder.

5.1.2 Wiring Capacity (W_c) Wiring capacity (W_c) is the most common definition of PWB density.

This connectivity definition expresses the interconnection capability of a substrate type.

It is established by determining the total length of conductors per square area of substrate (cm/cm^2 [in/in^2]), and is the total length of all conductors in all layers of the substrate divided by the area.

5.2 Design Basics

5.2 Design Basics Channel width and conductors per channel are design layout terms that refer to the distance between vias and/or component lands (channel width) and the maximum number of conductors that can be routed through each channel (conductors per channel). The feature pitch (center-to-center distance) and the size of the feature (annular ring or land size) define the channel width (see Figure 5-2 for these dimensions). The number of conductors per channel is determined by the channel width and

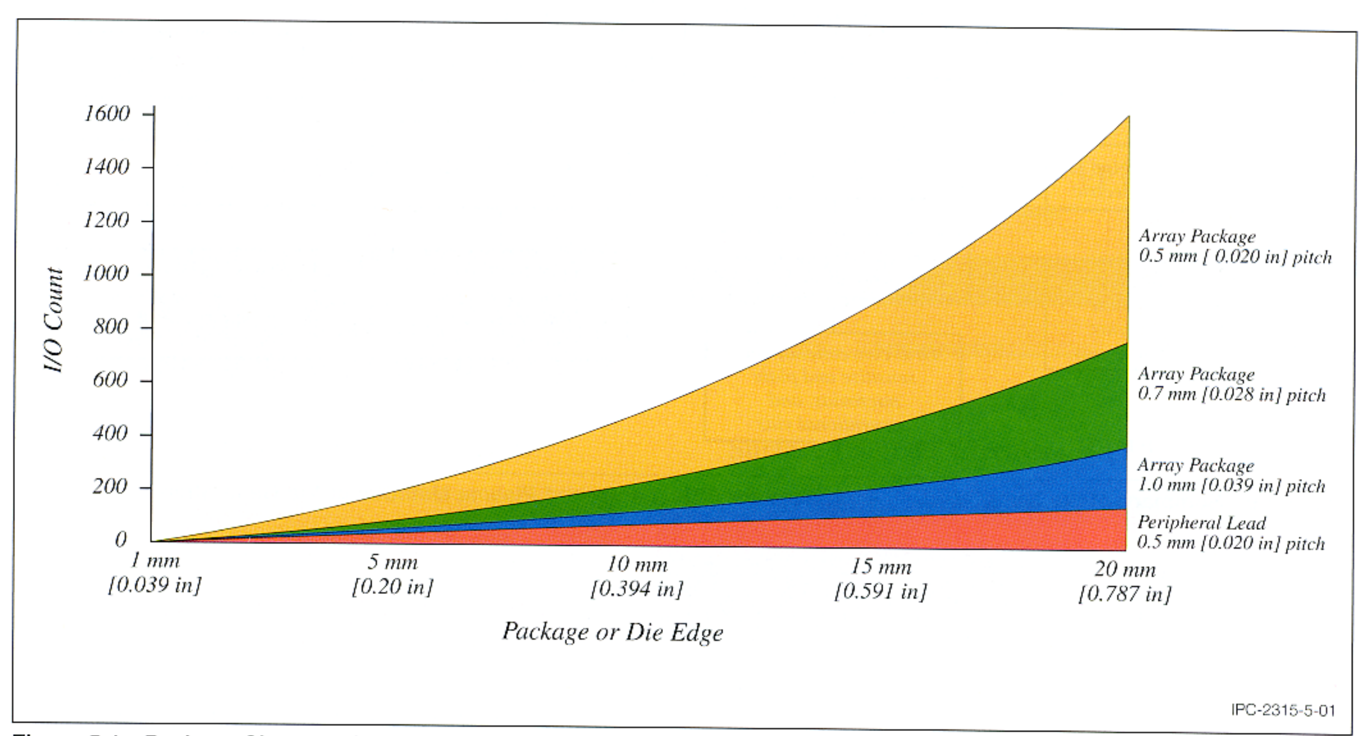


Figure 5-1 Package Size and I/O Count

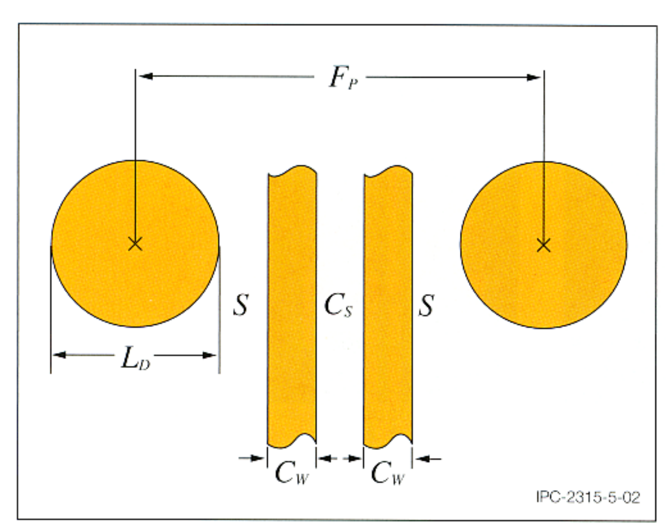


Figure 5-2 Feature Pitch and Feature Size Defining Channel Width

conductor width and spacing required to meet the electrical performance of the circuit(s).

It is important to note that the land size for a microvia feature is determined, rather than simply selected, as discussed in the following.

Manufacturers successfully use a wide variety of dielectrics for microvia boards, ranging from conventional glass-reinforced epoxy to ultra-thin unreinforced materials such as resin coated copper (RCC). The product's end-use environment and expected operating life, plus certain needed board-level attributes (e.g., dielectric withstand voltage, resin content to fill buried vias or avoid resin starvation, etc.) may require a particular dielectric type and/or thickness for the microvia layer. However, before the microvia diameter can be determined, the designer must select the thickness and type of dielectric for the microvia layer of the board to be built.

In addition, a suitable value for the aspect ratio of the blind microvia is also needed. The aspect ratio is the ratio of the length of the hole to the diameter of the hole (L/D). Acceptable values for aspect ratio are somewhat board vendor dependent and indicative of the hole configuration the vendors can form and plate reliably and consistently. At the time this document was prepared, typical aspect ratios range from about 0.5 to 0.85, although much effort is being expanded to push this value above 1.0 (see Section 7).

Outer foil thickness should be known or estimated.

The required as-formed diameter of the microvia is calculated as shown in Equation 1.

Microvia Diameter = $(j + f)/(A_r)$ [Equation 1]

Where:

j = Dielectric thickness on RDL
f = Outer foil thickness
A_r = Aspect ratio

The target pad and capture pad diameters are determined by adding two annular ring widths and a fabrication allowance to the as-formed diameter of the microvia. The required fabrication allowance is a function of material behavior and fabrication process tolerances. See Section 7 for further explanation.

It is important to consider these factors before conducting the wiring assessment to ensure realistic results for the type of board to be fabricated. Also note that conductor width and spacing (and required dielectric thickness) discussed in Section 6 and Section 7 may not be the same for Type I and Type II boards, due to plating performed on layer 2 and layer n-1 in the Type II board (see 7.1.2).

Examples of various feature pitch and conductors per channel combinations are shown in Figure 5-3, Figure 5-4, Figure 5-5, Figure 5-6, Figure 5-7, and Figure 5-8.

5.3 Determining the Number of Conductors Use Equation 2 to determine the number of conductors that can be used based on feature pitch.

Number of Conductors (C_N) =
$(F_p - Ld - 2s + Cs) / Cw + C_s)$ [Equation 2]

When C_S = S, the equation simplifies to Equation 3.

$C_N = [Fp - Ld - Cs] / (Cw + C_S)$ [Equation 3]

Where:

Fp = Feature pitch
Ld = Land diameter
Cs = Conductor spacing
Cw = Conductor width
s = Spacing between conductor and land

Table 5-1, Table 5-2, Table 5-3, Table 5-4, and Table 5-5 cover various feature pitch, land diameters, and conductor widths and spacings and give the number of conductors per channel width. Designers can interpolate for land diameters and line/space widths not listed. When using an autorouter, the fraction of a conductor is useable. When using a gridded CAD system, the fraction must be rounded down to the closest whole number.

5.4 Wiring Factor (W_f) Wiring factor is the actual density of a board resulting from the wiring distance required to connect all the electrical terminations of all the components, terminations, and test points on a board divided by the routable area. Wiring factor can be determined using Equation 4.

Wiring Factor (W_f) = εW_C [Equation 4]

Where:

ε = Layout efficiency
W_C = Substrate wiring capacity

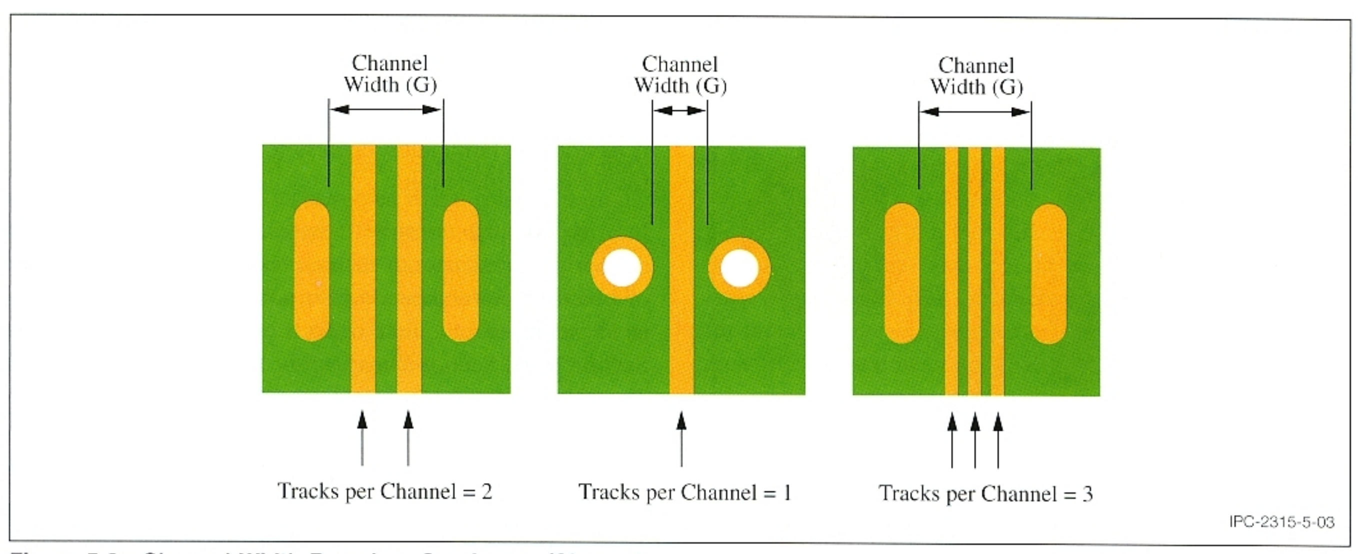


Figure 5-3 Channel Width Based on Conductors/Channel

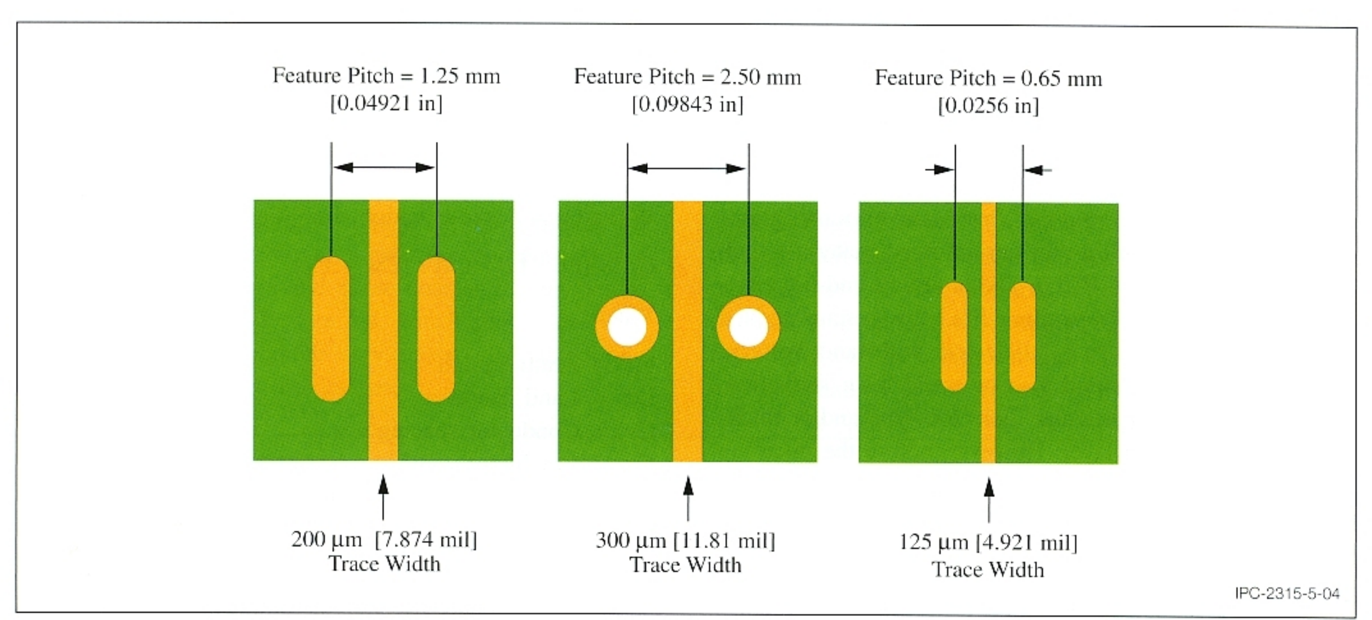


Figure 5-4 One Conductor/Channel Feature Pitches

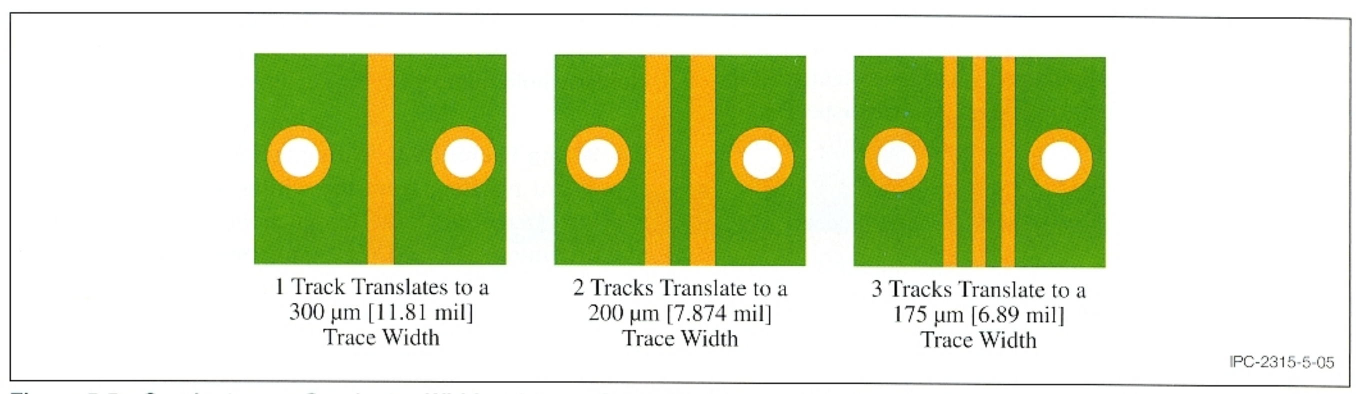


Figure 5-5 Conductor vs. Conductor Width – 2.5 mm [0.0984 in] Feature Pitch and 1.25 mm [0.04921 in] Land Width (Through-Hole Component)

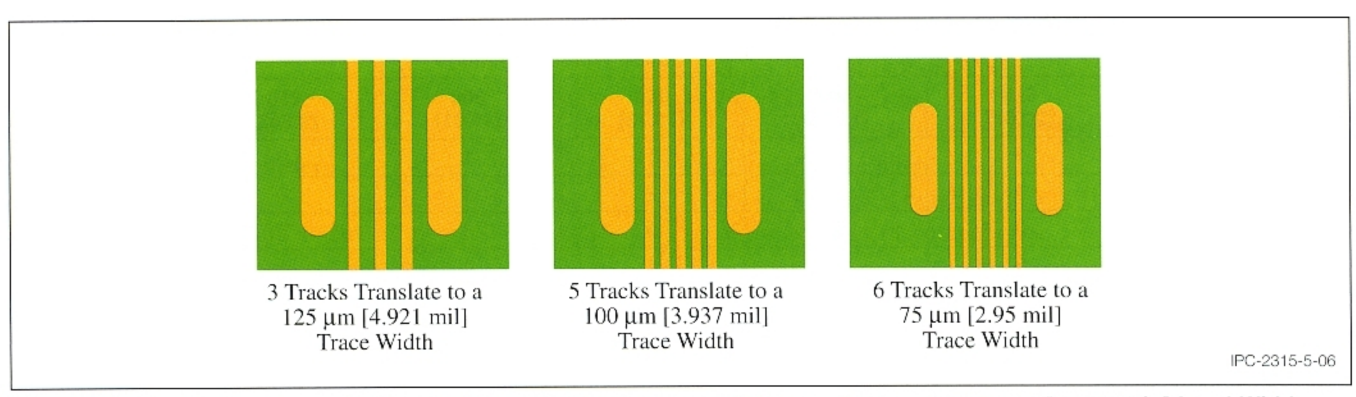


Figure 5-6 Conductor vs. Conductor Width – 1.25 mm [0.04921 in] Feature Pitch and 0.15 mm [0.00591 in] Land Width

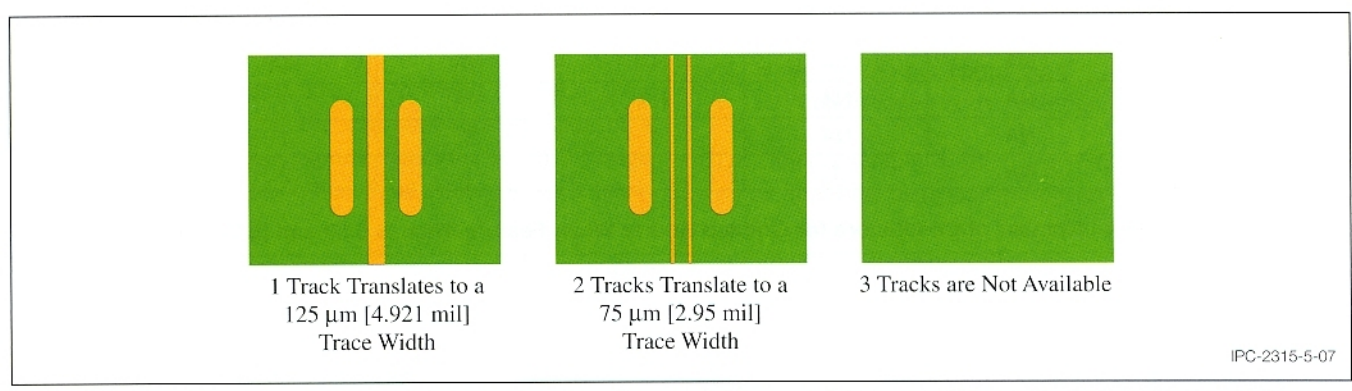


Figure 5-7 Conductor vs. Conductor Width – 0.65 mm [0.0256 in] Feature Pitch and 0.25 mm [0.00984 in] Land Width

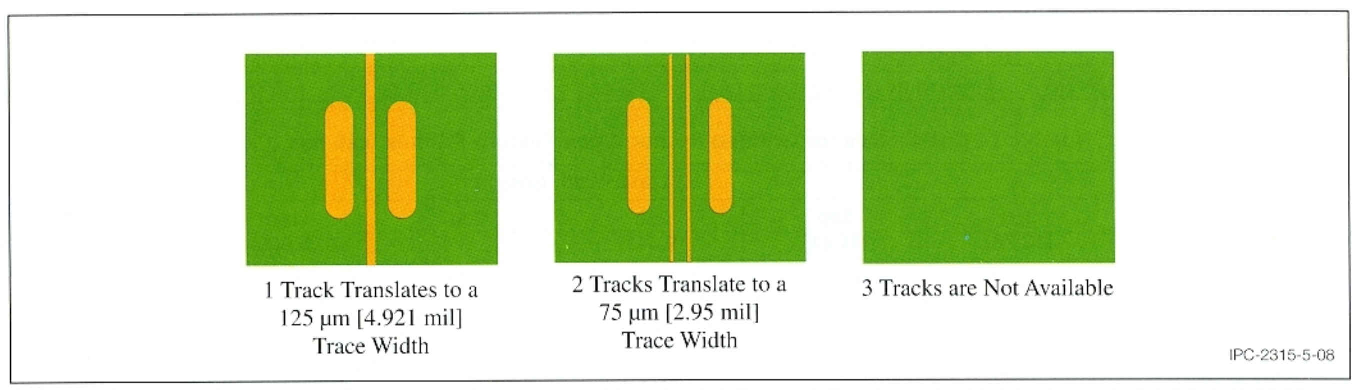


Figure 5-8 Conductor vs. Conductor Width – 0.50 mm [0.0197 in] Feature Pitch and 0.125 mm [0.004921 in] Land Width

Table 5-1 Number of Conductors for Gridded Router When Feature Pitch is 2.5 mm [0.0983 in]

Conductor Spacing and Width µm [mil]	Land Width µm [mil]					
	525 [20.67]	400 [15.75]	350 [13.78]	300 [11.81]	250 [9.843]	200 [7.874]
200 [7.874]	4	4	4	5	5	5
150 [5.906]	6	6	6	6	7	7
125 [4.921]	7	7	8	8	8	8
100 [3.937]	9	10	10	10	10	11
75 [2.95]	12	13	13	14	14	14

Table 5-2 Number of Conductors for Gridded Router When Feature Pitch is 1.25 mm [0.04921 in]

Conductor Spacing and Width (µm) [mil]	Land Width (µm) [mil]					
	525 [20.67]	400 [15.75]	350 [13.78]	300 [11.81]	250 [9.843]	200 [7.874]
200 [7.874]	1	1	1	1	2	2
150 [5.906]	1	2	2	2	2	3
125 [4.921]	2	2	3	3	3	3
100 [3.937]	3	3	4	4	4	4
75 [2.95]	4	5	5	5	6	6

Table 5-3 Number of Conductors for Gridded Router When Feature Pitch is 0.65 mm [0.0256 in]

Conductor Spacing and Width (µm) [mil]	Land Width (µm) [mil]					
	525 [20.67]	400 [15.75]	350 [13.78]	300 [11.81]	250 [9.843]	200 [7.874]
200 [7.874]	NA	NA	NA	NA	NA	NA
150 [5.906]	NA	NA	NA	NA	NA	1
125 [4.921]	NA	NA	NA	NA	1	1
100 [3.937]	NA	NA	1	1	1	1
75 [2.95]	NA	1	1	1	2	2

Table 5-4 Number of Conductors for Gridded Router When Feature Pitch is 0.50 mm [0.0197 in]

Conductor Spacing and Width (µm) [mil]	Land Width (µm) [mil]					
	400 [15.75]	350 [13.78]	300 [11.81]	250 [9.843]	200 [7.874]	150 [5.906]
200 [7.874]	NA	NA	NA	NA	NA	NA
150 [5.906]	NA	NA	NA	NA	NA	NA
125 [4.921]	NA	NA	NA	NA	NA	NA
100 [3.937]	NA	NA	NA	NA	1	1
75 [2.95]	NA	NA	NA	1	1	1
50 [1.97]	NA	1	1	2	2	3

Table 5-5 Number of Conductors for Gridded Router When Feature Pitch is 0.25 mm [0.00984 in]

Conductor Spacing and Width (µm) [mil]	Land Width (µm) [mil]					
	350 [13.78]	300 [11.81]	250 [9.843]	200 [7.874]	150 [5.906]	100 [3.937]
150 [5.906]	NA	NA	NA	NA	NA	NA
125 [4.921]	NA	NA	NA	NA	NA	NA
100 [3.937]	NA	NA	NA	NA	NA	NA
75 [2.95]	NA	NA	NA	NA	NA	NA
50 [1.97]	NA	NA	NA	NA	NA	1

There are three cases that drive the wiring factor:

1. Escape from a component (like CSP or component; see 5.4.1).
2. Wiring between two or more tightly linked components (like a CPU and cache; see 5.4.2).
3. Demand produced by all components on both sides of an assembly (see 5.4.3).

5.4.1 Localized Escape Calculations Component land patterns can be peripheral or full array. Peripheral arrays are the most practical for using leading edge HDI design rules.

5.4.1.1 Full Array Equation 5 can be used for predicting the number of signal layers for breakout of a particular group of I/Os on a component as seen below. In 1992, Dr. Clinton Chao, HP Laboratories, first developed this equation.

[Equation 5]

$$\text{Number of Signal Layers} = \left[\frac{[n/2]-[(G-D_b-C_s)/(C_w+C_s)]+1}{[(G-D_v-C_s)/(C_w+C_s)]+1}\right]_{INT.} + 1$$

Where:

C_w = Conductor width
C_s = Conductor spacing
D_v = Via land diameter
D_b = Contact land diameter
G = I/O pitch
n = No. of rows in full square array

5.4.1.2 Peripheral Array The general equation for peripheral array components is similar to that for area array. It requires only the substitution of the term 'r' (r = the number of rows deep of contacts) for the n/2 term in Equation 5. The chip or package will be larger than a full array, but the design rules and number of signal layers will be much less aggressive.

Table 5-6 displays the number of pad rows that can escape from a full or peripheral array component per HDI layer using blind microvias. If the chip and substrate size of a peripheral array can be accommodated, the reduced design rules and layer count has a beneficial effect on PWB fabrication costs.

5.4.2 Wiring Between Tightly Linked Components

Equation 6 shows how to calculate tightly linked components.

$$W_C = \frac{(2.5)(N_t)(P_N - 1) R}{(P)(P_N)(\varepsilon)} \qquad \text{[Equation 6]}$$

Where:

N_t = I/Os per component
P_N = Leads per net
ε = Wiring efficiency (30% to 80%)
P = Module pitch
R = Average wiring length = $k(1+0.1 \ln N)N^{1/6}$ – k=0.75
N = Number of components

Figure 5-9 gives a visual example of this equation. This equation can be simplified. The wiring factor (cm/cm^2) [in/in sq.] can now be determined using Equation 7.

$$W_C = 2.25\ (P \times N_t) \qquad \text{[Equation 7]}$$

Where:

N_t = No. of I/O per component
P = Pitch between active components

Dr. Donald Seraphim, IBM, made such a derivation (based on an empirical analysis) and observed that it is impossible to fill all available wiring channels with conductors. The empirically established efficiency, ε, is between 25% and 70%. Fifty percent efficiency is normally used, thus the maximum available wiring capacity (connectivity) must be twice the length of the necessary or actually required wiring (wiring factor).

Table 5-6 Pad Rows that can Escape per HDI Layer for Different Feature Sizes

Trace/Space (µm) [mil]	Pad Diameter (cm) [in]	Component Pitch Size (mm) [in]					
		1.15 [0.04528]	1.0 [0.0394]	0.80 [0.0315]	0.75 [0.0295]	0.65 [0.0256]	0.50 [0.0197]
75 [2.95]	0.025 [0.009842]	6	5	4	3	3	2
	0.030 [0.01181]	6	5	3	3	2	1
	0.035 [0.01378]	5	4	3	3	2	1
	0.040 [0.01575]	5	4	3	2	2	1
100 [3.937]	0.025 [0.009842]	4	4	3	2	2	1
	0.030 [0.01181]	4	3	2	2	2	1
	0.035 [0.01378]	4	3	2	2	1	1
	0.040 [0.01575]	4	3	2	2	1	1
125 [4.921]	0.025 [0.009842]	4	3	2	2	2	1
	0.030 [0.01181]	3	3	2	2	1	1
	0.035 [0.01378]	3	3	2	2	1	1
	0.040 [0.01575]	3	2	2	1	1	1

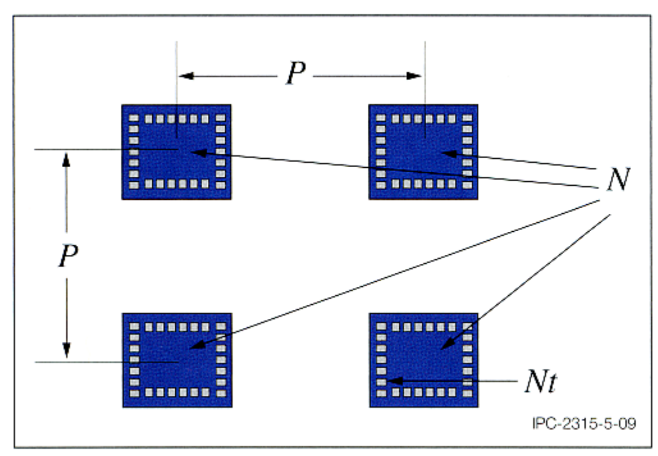


Figure 5-9 Wiring Factor Model for Tightly Coupled Components

5.4.3 Total Wiring Requirements As a general rule, the escape routing from microcomponents does not exclusively determine the design rules or number of signal layers. Other factors such as the printed wiring assembly form factor, the pitch of the other SMT components, how many parts are on the back side, and the distance between parts may drive the need for different design rules and more signal layers than those required by the pin out of the microcomponents alone.

The easiest equation to use is the wiring density (W_D) predictor given in Equation 8, which relates to the total parts on both sides of an assembly, the assembly area, total number of leads, and a factor relating the semiconductor technology being used.

$$W_D = \beta\sqrt{(p/a)} \bullet (l/p) \quad \text{[Equation 8]}$$

Where:

p = Total parts on both sides of an assembly
a = Area on an assembly (one surface only)
l = Total leads of all parts including connector fingers
β = 2.5 (analog & digital, high discrete)
β = 3.0 (digital products)
β = 3.5 (high ASIC focus, MCM, PCMCIA)

This wiring density (W_D) is the actual wiring in cm/cm^2 that an average of three nodes per net would require for the parts (p) with leads (l) on a PWB area (a).

This is related in the equation for wiring factor (see Equation 3).

To convert the wiring factor into a series of layer count and design rule combinations that will satisfy the density requirements of the proposed HDI design, the PWB layout system efficiency is divided into the wiring factor. PWB CAD layout efficiency is estimated from benchmarking actual designs and is only an approximation. Each designer, CAD system, and placement methodology will affect the routing efficiency.

Table 5-7 shows the estimated efficiencies (ε) that can be used for various design combinations.

5.5 Via and Land Density Higher via density conflicts with higher conductor density. However, it is not the via itself that causes the conflict; it is the land required for the via. This is because the via land and conductor pattern occupy the same routing surface on the layer. The land is the locus of position the via could have considering all the fabrication and material tolerances. So the via can become increasingly smaller and the land will still be needed, a compromise must exist between the number of via/land sites on the PWB and the conductor density. For example, a feature pitch of 1.25 mm [0.04921 in] permits a maximum of 64 vias/cm^2 [163 vias/in^2], a pitch of 0.65 mm [0.0256 in] permits 225 vias/cm^2 [572 vias/in^2], and a pitch of 0.50 mm [0.0197 in] permits 400 vias/cm^2 [1016 vias/in^2].

5.6 Trade Off Process

5.6.1 Wiring Factor Process Figure 5-10 gives an example of a wiring process flow chart.

5.6.2 Input/Output (I/O) Variables The input variables for the trade off formulas are given in Equation 9, Equation 10, Equation 11, Equation 12, Equation 13, and Equation 14.

Parts per square area (PPA) = p ÷ s [Equation 9]

Average leads per part (LPP) = l ÷ p [Equation 10]

$$W_D = 3.5\,(\sqrt{PPA}) \times LPP \quad \text{[Equation 11]}$$

$$W_C = W_D \div P_L \quad \text{[Equation 12]}$$

Where:

P_L = PWB layout efficiency - The percentage of wiring capacity the wiring factor consumes.

Number of layers (L) = (W_c x G) ÷ C_N [Equation 13]

Where:

G = Channel width - The width of the space between adjacent via holes or component lands with which to run conductors.

Number of Conductors (C_N) = (W_C x G) ÷ L [Equation 14]

Where:

L = Signal layers - The number of PWB layers dedicated to running conductors (does not include power or ground layers).

5.7 Typical Examples Some typical HDI design examples are given in 5.7.1 through 5.7.3 and offer examples of HDI design for direct chip attach, blind vias with SMT, and fine pitch SMT.

Table 5-7 Efficiencies

Design Scenario	Conditions	Efficiency (ε) (%)
Normal Rigid	Through-hole SMT with/without back side passives (gridded CAD)	25
Normal Rigid	Through-hole SMT with/without back side passives (gridded CAD)	45
Normal Rigid	Through-hole SMT with back side active component (gridded CAD)	40
Normal Rigid	One side blind vias (using autorouter)	60
Normal Rigid	Two side blind vias (using autorouter)	70
Two-Layer Redistribution	Using autorouter	75
Four-Layer Redistribution	Using autorouter	80

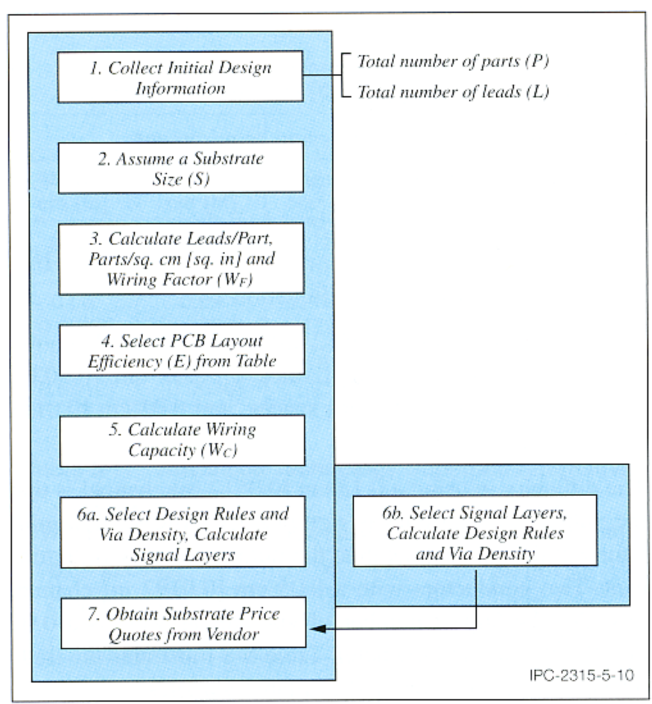


Figure 5-10 Wiring Process Flow Chart

5.7.1 Case I – HDI With Direct Chip Attach Figure 5-11 displays an example of HDI with a direct chip attach.

Proposed HDI Portable Design:
Overall Size: 7.5 cm x 4.0 cm [2.95 in x 1.57 in]
Number of Components: 495
Total Number of Leads: 1610
Size = 7.5 cm x 4.0 cm, 30 cm^2, 2 gm [2.95 in x 1.57 in, 4.63 in^2, 0.0705 oz]

Step A: Collect Initial Design Information

Purpose of this step: To ensure all design information to perform an advanced substrate design trade off is available.

Number of components or devices: The total number of components to be assembled on either side of the board.

Number of component leads: The total number of leads (or I/Os) of the components in item 1.

For the proposed advanced substrate design, the values of the design inputs are:

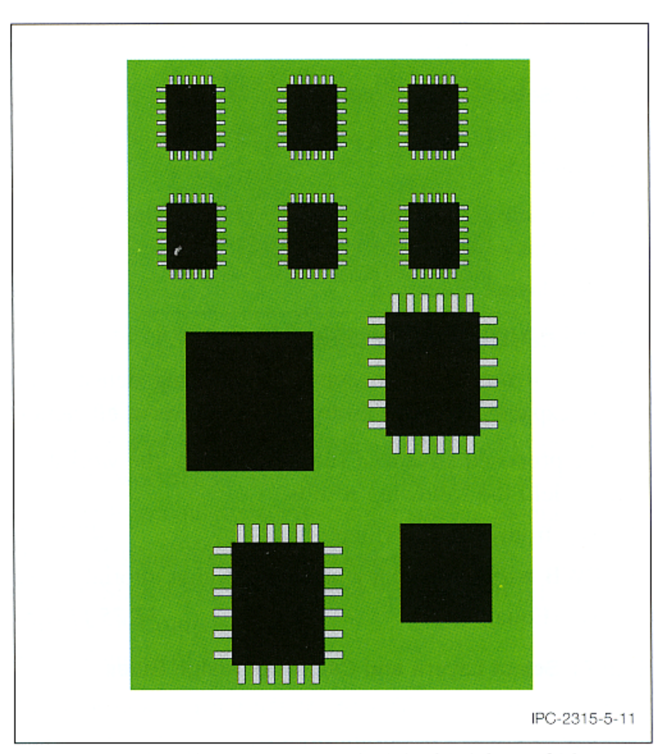


Figure 5-11 Typical Example of HDI with Direct Chip Attach

1. Total number of parts *495*
2. Total number of leads (I/Os) *1610*

Step B: Assume a Board Size

Purpose of this step: To capture or allow the selection of an optimal size of the assembly to be designed.

Overall size: The projected size of the PWB area minus any keep-out areas where conductor routing is not permitted.

Assume an overall maximum dimension of the substrate. Although the overall size is best assumed to be a rectangular box, non-uniform sizes can be incorporated. Use the exact area if known. The rectangular box dimensions will be used later for pricing purposes.

Overall size = 7.5 cm x 4.0 cm [2.95 in x 1.57 in]

For the proposed advanced substrate design, the values for the size are:

3. Substrate size cm^2 [in^2] *30 [4.63]*

Step C: Calculate Substrate Metrics and Wiring Density

Purpose of this step: To calculate the two key metrics that are used to calculate the overall measure of circuit density and wiring factor. The wiring density will subsequently be used to estimate the required wiring capacity.

The following worksheet will be used to calculate the wiring density:

4. Parts per area (cm^2) [in^2] (Equation 9) *17 [107]*
5. Average leads per part (Equation 10) *3.25*
6. W_D from Equation 8 *47 [118]*

Step D: Select Layout Efficiency

Purpose of this step: To select a PWB layout efficiency from Table 5-7.

We have selected a four-layer HDI construction. The layout efficiency from Table 5-7 is 0.8.

7. PWB layout efficiency *0.8*

Step E: Calculate Wiring Capacity

Purpose of this step: To convert the wiring density into wiring capacity by dividing by the PWB layout efficiency.

For the proposed advanced substrate design, the worksheet would yield the following results:

8. W_D from trade off (Step C) *47 [118]*
9. PWB wiring efficiency based on design tutorial *0.8*
10. W_c (Equation 12) *58.75 [147.5]*

Step F: Select Layers and Calculate Design Rules

Purpose of this step: To convert the wiring capacity to an estimate of a series of design rules by fixing the layer count and using Equation 7.

From Step E, it was determined that the wiring capacity for the proposed design in Figure 5-10 is 58.75 [147.5]. If it is designed as a four layer HDI with two signal layers, the required number of conductors utilizing a 0.05 cm [0.0197 in] channel width would be:

11a. Signal layers based on design requirements 2

12a. W_C from trade off (Step E) *58.75 [147.5]*

13a. Channel width (G) (cm [in]) based on design requirements *0.05 [0.0197]*

14a. Conductors per channel (Equation 14) *1.5*

The derived number of conductors is always rounded-off to the nearest integer value. Therefore, the number of conductors of 1.5 rounded-off to two, or two conductors per 0.05 cm [0.0197 in] channel.

If the proposed design in Figure 5-10 was designed using a 0.06 cm [0.0236 in] channel width, the number of conductors per channel would be:

11b. Signal layers based on design requirements 2

12b. W_C from trade off (Step E) *58.75 [147.5]*

13b. Channel width (G) (cm [in]) based on design requirements *0.06 [0.0236]*

14b. Conductors per channel (Equation 14) *1.8*

The derived number of conductors is always rounded up to the nearest integer value. Therefore, the number of conductors of 1.8 rounded off to two. Therefore, the use of a 0.06 cm [0.0236 in] channel would require two conductors per channel.

If further calculations were performed using a channel width of 0.13 cm [0.0512 in], the number of conductors per channel would be:

Step G: Trade Off Process

15. Signal layers based on design requirements 2
16. W_C from trade off (Step E) *58.75 [147.5]*
17. Channel width (cm [in]) based on design requirements *0.13 [0.0512]*
18. Conductors per channel (Equation 14) *3.8*

Therefore, a 0.13 cm [0.0512 in] channel would require four conductors with design rules of 0.01 cm [0.0039] lines, 0.013 cm [0.005118 in] spaces, and 0.03 cm [0.0118 in] via lands.

The difficulty in using a 0.13 cm [0.0512 in] channel is that the number of microvias is significantly reduced. In a miniaturized design such as this, the number of vias is significant. Two conductors with a 0.05 cm [0.0197 in] channel provides the largest number of via sites as well as a 0.02 cm [0.0079 in] land diameter. Table 5-8 illustrates the trade off between conductors and available via sites.

Table 5-8 Conductors Per Channel (Two Conductors; Assumes 0.03 cm [0.012 in] Land Size)

Channel Width cm [in]	Feature Pitch cm [in]	Via Sites Per cm^2 [in^2]	Signal Layers
0.05 [0.0197]	0.08 [0.0315]	156 [1006]	2
0.06 [0.0236]	0.09 [0.0354]	123 [796]	2
0.13 [0.0512]	0.16 [0.0630]	39 [252]	2

Each signal layer and conductor combination represents a separate design alternative for the proposed HDI design. The number of power and ground planes is subsequently added to the signal layer count to determine the total number of layers for each alternative. In this example, there is just a ground plane.

With the addition of one or more power or ground planes, the total layer count for each alternative is then as shown in Table 5-9.

Using Table 5-1, Table 5-2, Table 5-3, Table 5-4, and Table 5-5, the three design alternatives can be presented in terms of total number of layers and design rules (see Table 5-10 and Table 5-11).

Table 5-9 Number of Conductors Per Channel (Two Conductors; Assumes 0.020 cm [0.00787 in] Land Size)

Channel Width cm [in]	Feature Pitch cm [in]	Signal Layers	Plane Layers	Total Layers	Via Sites Per cm² [in²]	Maximum Land Diameter (μm) [mil]
0.05 [0.0197]	0.07 [0.0276]	2	2	4	204 [1316]	200 [7.874]
0.06 [0.0236]	0.087 [0.03425]	2	2	4	132 [852]	270 [10.63]
0.13 [0.0512]	0.16 [0.0630]	2	2	4	39 [252]	300 [11.81]

Table 5-10 Advanced Design Rules (Assumes 0.027 cm [0.010630 in] Land Size)

Channel Width cm [in]	Feature Pitch cm [in]	Via Sites Per cm² [in²]	Total Layers	Width of Conductors and Spaces (μm) [mil]
0.05 [0.0197]	0.08 [0.0315]	156 [1006]	4	80/80 [3.150/3.150]
0.06 [0.0236]	0.09 [0.0354]	123 [796]	4	80/80 [3.150/3.150]
0.13 [0.0512]	0.16 [0.0630]	39 [252]	4	100/120 [3.937/4.724]

Table 5-11 Advanced Technology Substrate Alternative

Channel Width (cm) [in]	Total Layers	Design Rules (μm) [mil]
0.05 [0.0197]	4	80 [3.150]
0.06 [0.0236]	4	80 [3.150]
0.13 [0.0512]	4	100 [3.937]

Step H: Document

Purpose of this step: This information may now be provided with all other required substrate pricing information (e.g., order volume, metallization types, electrical test requirements, etc.) to a PWB account manager.

5.7.2 Case II – Drilled Blind Via With SMT Alternative in wiring density due to blind vias on FR-4 substrates with conventional SMT Parts, CASE 2. See Figure 5-12 for an example of blind vias with SMT parts.

Since blind vias do not pass through the entire PWB; they only require one outerlayer land per via (as opposed to two for each through via). This reduction in land demand can lead to an increase in the amount of available outerlayer space for additional components and/or outerlayer conductors, leading to an overall increase in circuit density. However, this increase in density may not be significant enough to lead to a reduction in layer count.

The wiring factor introduced in Step B of the trade off process will be used to determine if the use of blind vias will lead to a reduction in layer count. The effect of blind vias will be addressed through the use of an increased value for

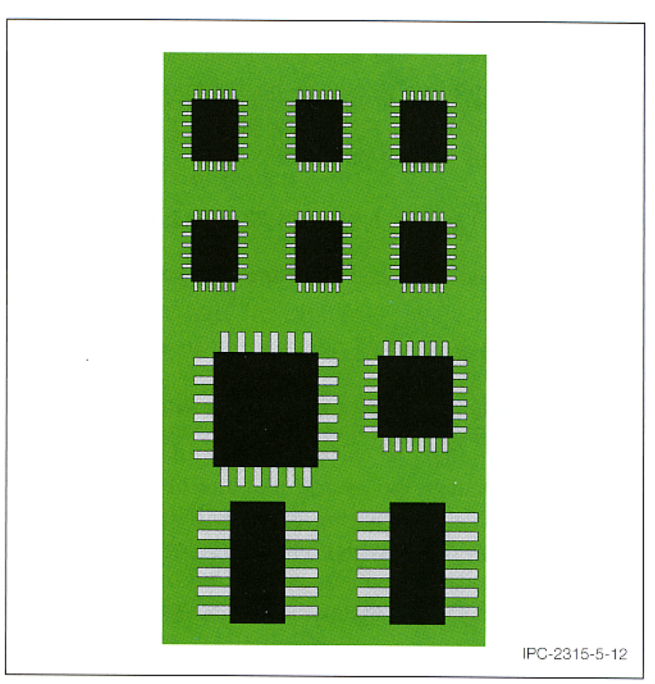


Figure 5-12 Example of Drilled Blind Via With SMT

wiring efficiency [60% (one sided) and 70% (two sided) instead of 45% for conventional rigid boards] in the wiring capacity worksheet. The size of the substrate has been changed to accommodate the larger surface mount parts.

Proposed Blind Via Portable Design:
Overall Size: 12 cm x 6.0 cm [4.72 in x 2.36 in]
Number of Components: 495
Total Number of Leads: 1610

The new design information is:

Size = 12 cm x 6 cm, 72 cm², 21 gms. [4.72 in x 2.36 in, 11.14 in², 0.741 oz]

Step A: Collect Initial Design Information

Purpose of this step: To ensure all design information to perform an advanced substrate design trade off is available.

Number of components or devices: The total number of components to be assembled on either side of the board.

Number of component leads: The total number of leads (I/Os) of the components in item 1.

For the proposed advanced substrate design, the values of the design inputs are:

1. Total number of parts *495*
2. Total number of leads (I/O) *1610*

Step B: Assume a Board Size

Purpose of this step: To capture or allow the selection of an optimal size of the assembly to be designed.

Overall size: The projected size of the PWB area (L X W) minus any keep-out areas where conductor routing is not permitted.

Assume an overall maximum dimension of the substrate. Although the overall size is best assumed to be a rectangular box, non-uniform sizes can be incorporated. Use the exact area if known. The rectangular box dimensions will be used later for pricing purposes.

Overall size = 12 cm x 6.0 cm [4.72 in x 2.36 in]

For the proposed advanced substrate design, the values for the size are:

3. Overall size (cm^2) [in^2] *72 [11.14]*

Step C: Calculate Substrate Metrics and Wiring Factor

Purpose of this step: To calculate the two key metrics that are used to calculate the overall measure of circuit density and wiring factor. The wiring factor will subsequently be used to estimate the required wiring capacity.

The following worksheet is used to calculate the wiring factor.

4. Parts per area (Equation 9) *8*
5. Average leads per part (Equation 10) *3.25*
6. W_F (Equation 8) *30 [75]*

Step D: Select Layout Efficiency

Purpose of this step: To select a PWB layout efficiency from Table 5-7.

For the proposed advanced substrate design (CASE 2), Table 5-7 would yield the following results for blind vias drilled from one side:

7a. PWB layout efficiency *0.6*

For the proposed Advanced Substrate Design (CASE 2), Table 5-7 would yield the following results for blind vias drilled in from two sides.

7b. PCB layout efficiency *0.7*

Step E: Calculate Wiring Capacity

Purpose of this step: To convert the wiring factor into wiring capacity by dividing by the PWB layout efficiency.

For the proposed advanced substrate design, the worksheet would yield the following results:

For blind vias drilled in from one side:

8a. W_F from trade off (Step C) *30 [75]*
9a. PWB wiring efficiency based on design tutorial *0.6*
10a. W_C (Equation 12) *50 [125]*

For blind vias drilled in from two sides:

8b. W_F from trade off (Step C) *30 [75]*
9b. PWB wiring efficiency based on design tutorial *0.7*
10b. W_c (Equation 12) *43 [107]*

Step F: Select Design Rules and Calculate Layers

Purpose of this step: To convert the wiring capacity to an estimate of a series of signal layers by fixing the conductors per channel and using Equation 12.

From Step E, it was determined the wiring capacity for the proposed design in Figure 5-2 is 50 cm/cm^2 [127 in/in^2] and 43 cm/cm^2 [109 in/in^2]. Utilizing a 0.25 cm [98.4 mil] channel width, the number of signal layers would be:

11. W_C from trade off (Step 10a and Step 10b) *50 / 43 [125 / 107]*
12. Channel width (cm) [in] based on design requirements *0.25 / 0.25 [0.0984 / 0.0984]*
13. Conductors per channel based on design requirements *3*
14. Signal layers (Equation 13) *4.2 / 3.6*
15. Rounded off signal layers *5 / 4*

With the addition of one ground plane, the total layer counts for each alternative will then be as shown in Table 5-12.

Table 5-12 Total Layer Counts and Alternatives

Layers	Blind Vias Drilled from One Side	Blind Vias Drilled from Two Sides
Signal Layers	5	4
Plane Layers	1	1
Total Layers	6	5

Using Table 5-1, Table 5-2, Table 5-3, Table 5-4, or Table 5-5, the two design alternatives can now be presented in terms of total number of layers, design rules, and blind via features, as shown in Table 5-13.

Table 5-13 Design Alternatives Based on Layers, Vias, and Design Rules

	Blind Vias Drilled from One Side	Blind Vias Drilled from Two Sides
Design Rules (μm) [mil]	130 [5.118]	130 [5.118]
Total Layers	6	5

Step G: Document

Based on the information provided in Table 5-13, the designer should then document the resulting criteria. Table 5-14 is an example of how the documentation may appear.

Table 5-14 Reporting Requirements Example HDI PWBs with Blind Vias

	Blind Vias from One Side	Blind Vias from Two Sides
Design Rules (cm) [in]	0.013 [0.00512]	0.013 [0.00512]
Total Layers	6	5

5.7.3 CASE III – Fine Pitch SMT Alternative in wiring factor due to conventional vias on FR-4 substrates with conventional SMT parts, CASE 3 (see Figure 5-13).

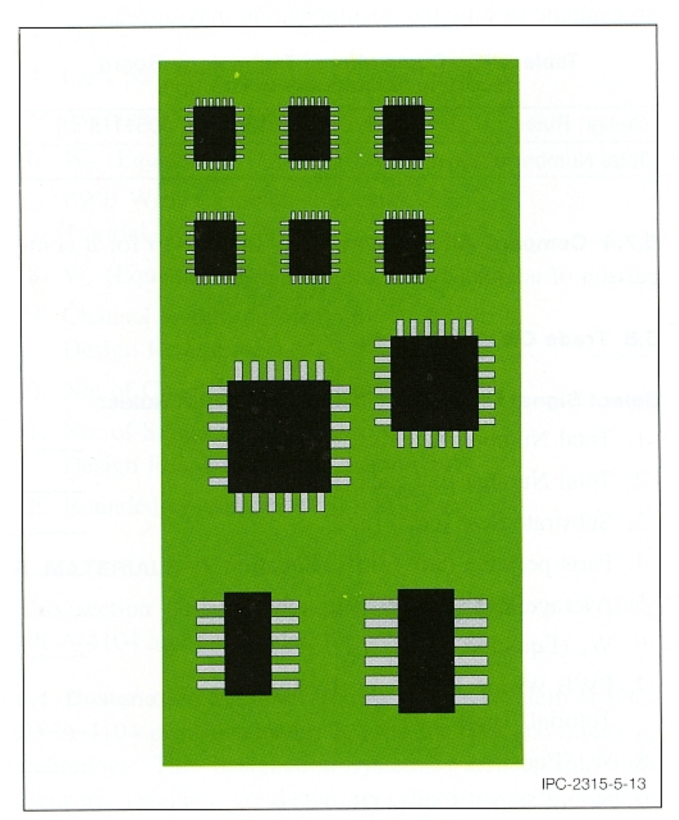


Figure 5-13 Example of Fine Pitch SMT

This is the conventional case of PWB design with vias.

The wiring factor introduced in Step 2 of the trade off process will be used to determine the layer count. The effect of vias will be addressed through the use of the conventional wiring efficiency of 25% in Table 5-7. The size of the substrate has been changed to accommodate the larger surface mount parts and the increased space required for via lands that go all the way through the board.

Proposed Conventional Design:
Overall Size: 15 cm x 7.5 cm [5.91 in x 2.95 in]
Number of Components: 495
Total Number of Leads: 1610

For the proposed design, the values of the design inputs are:

Size = 15 cm x 7.5 cm; 113 cm^2; 36 gms [5.91 in x 2.95 in; 17.73 in^2; 1.27 oz]

Step A: Collect Initial Design Information

Purpose of this step: To ensure all design information to perform an advanced substrate design trade off is available.

Number of components or devices: The total number of components to be assembled on either side of the board.

Number of component leads: The total number of leads (I/Os) of the components in item 1.

For the proposed advanced substrate design, the values of the design inputs are:

1. Total number of parts *495*
2. Total number of leads (I/O) *1610*

Step B: Assume a Board Size

Purpose of this step: To capture or allow the selection of an optimal size of the assembly to be designed.

Overall size: The projected size of the PWB area minus any keep-out areas where conductor routing is not permitted.

Assume an overall maximum dimension of the substrate. Although the overall size is best assumed to be a rectangular box, non-uniform sizes can be incorporated. Use the exact area if known. The rectangular box dimensions will be used later for pricing purposes.

Overall size = 15 cm x 7.5 cm [5.91 in x 2.95 in]

For the proposed advanced substrate design, the values for the size are:

3. Overall size (cm^2) [in^2] 113 [17.14]

Step C: Calculate Substrate Metrics and Wiring Factor

Purpose of this step: To calculate the two key metrics that are used to calculate the overall measure of circuit density; wiring factor. The wiring factor will subsequently be used to estimate the required wiring capacity.

The following worksheet will be used to calculate the wiring factor.

4. Parts per area (cm^2) [in^2] (Equation 9) *4.4 [28.9]*
5. Average leads per part (Equation 10) *3.25*
6. W_F from the W_F (Equation 8) *23.8 [61.15]*

Step D: Select Layout Efficiency

Purpose of this step: To select a PWB layout efficiency from Table 5-7.

For the proposed advanced substrate design (CASE 3), Table 5-7 would yield the following results for a conventional through-hole board using a gridded CAD system:

7. PWB layout efficiency based on design tutorial: *0.25*

Step E: Calculate Wiring Capacity

Purpose of this step: To convert the wiring factor into wiring capacity by dividing by the PWB layout efficiency.

For the proposed advanced substrate design, the worksheet would yield the following results:

6. W_F from trade off (Step 3) *23.8 [61.15]*
7. PWB wiring efficiency *0.25*
8. W_C (Equation 12) *95.2 [244.6]*

Step F: Select Design Rules and Calculate Layers

Purpose of this step: To convert the wiring capacity to an estimate of a series of signal layers by fixing the conductors per channel.

According to Step E, the wiring capacity for the proposed design in Figure 5-2 is 95.2 cm/cm^2 [244.6 in/in^2]. Utilizing a 0.25 cm [0.0984 in] channel width, the number of signal layers would be:

8. W_C from trade off (Step E)	*95.2 [244.6]*
9. Channel width (cm) [in] based on design requirements	*0.25 [0.0984]*
10. Conductors per channel based on design requirements	*6*
11. Signal Layers (Equation 13)	*3.9 [4.0]*
12. Rounded off signal layers	*4 [4]*

With the addition of two ground/power planes, the total layer counts for each alternative then becomes:

Number of signal layers	*4*
Number of plane layers	*2*
Total number of layers	*6*

Using the conductors per channel-to-design rules conversion table (see 5.3), the design alternatives can now be presented in terms of total number of layers, design rules, and features:

Design rules (conductor width, land diameter) *0.013 cm [0.005118 in] / 0.069 cm [0.02717 in]*

Total number of layers *6*

Step G: Document

Based on the information provided in Step 6, the designer should then document the resulting criteria. Table 5-15 is an example of how the documentation may appear:

Table 5-15 Conventional Technology Board Reporting Requirements Example

Design Rules	0.013 cm [0.0051118 in]
Total Number of Layers	6

5.7.4 Compare Alternatives See Table 5-16 for a comparison of advanced technology alternatives.

5.8 Trade Off Worksheets

Select Signal Layers and Calculate Design Rules:

1. Total Number of Parts ____
2. Total Number of Leads (I/O) ____
3. Substrate Size (cm^2) [in^2] ____
4. Parts per area (cm^2) [in^2] (Equation 9) ____
5. Average leads per part (Equation 10) ____
6. W_F (Equation 8) ____
7. PWB Wiring Efficiency (Design Tutorial, Table 5-7) ____
8. W_c (Equation 12) ____
9. No. of Signal Layers (Based on Design Requirements) ____
10. Channel Width (cm) [in] (Based on Design Requirements) ____
11. No. of Conductors per Channel (Equation 14) ____

Table 5-16 Advanced Technology Alternatives

	Conventional PWB	Blind Via PWB	Microvia HDI PWB
Channel Width (cm/cm) [in/in]	0.25/0.25 [0.984/0.984]	0.25/0.25 [0.984/0.984]	0.60/0.50 [0.0236/0.0197]
Size of Substrate (cm^2) [in^2]	116/69 [45.67/27.2]	69/29 [27.2/11.4]	30/30 [4.63/4.63]
Weight of Substrate (gm.) [oz]	36/21 [1.27/0.741]	21/2 [1.27/0.071]	2/2 [0.071/0.071]
Density (cm/cm^2) [in/0.0155 in^2]	23.6/30 [9.291/11.8]	30/47 [11.8/18.5]	47/47 [118/118]
Design Rules (μm) [mil]	130/130 [5.118/5.118]	130/100 [5.118/3.937]	80/80 [3.150/3.150]
Via Land Size (μm) [mil]	700/700 [27.56/27.56]	700/300 [27.56/11.81]	270/200 [10.63/7.874]
Total Number of Layers	6/6	5/4	4/4
Blind Vias	No/1 Sided	2 Sided/Yes	Yes/Yes
Microvia Substrate	No/No	No/Yes	Yes/Yes
Via Density (# per cm^2) [0.0155 in^2]	16/16	16/64	121/196

Select Design Rules and Calculate Signal Layers:

1. Total Number of Parts ____
2. Total Number of Leads (I/O) ____
3. Substrate Size (cm^2) [in^2] ____
4. Parts per area (cm^2) [in^2] (Equation 9) ____
5. Average leads per part (Equation 10) ____
6. W_F (Equation 8) ____
7. PWB Wiring Efficiency (Design Tutorial, Table 5-7) ____
8. W_c (Equation 12) ____
9. Channel Width (cm) [in] (Based on Design Requirements) ____
10. No. of Conductors per Channel ____
11. No. of Signal Layers (Based on Design Requirements) (Equation 14) ____
12. Rounded up number of Signal Layers ____

6 MATERIALS

This section describes the classification scheme of IPC/JPCA-4104 and is intended for reference only.

6.1 Designation System The designation system of IPC/JPCA-4104 identifies materials used for HDI and microvia technology. This designation system, which is split into dielectric insulator, conductor, and dielectric with conductors, provides specific codes for materials type, form of dielectric, reinforcement, chemistry, etc. for ordering purposes.

Each specification sheet in IPC/JPCA-4104 outlines engineering and performance data for HDI and microvia materials. The specification sheets are provided with letters and numbers for identification purposes. For example, if a user wishes to order from the specification sheet number 1, the number "1" would be used when placing the order (i.e., IPC/JPCA-4104/1).

6.2 Application Level Recognizing the fact HDI materials may be subject to grouping by specific level of application, IPC/JPCA-4104 divides HDI materials into three application levels.

H – PWB/HDI Applications
I – IC Packaging Applications
U – User defined

7 CLASSIFICATION OF PRODUCTS

7.1 Structure The design designation system of this document recognizes six general structure types used in the design of HDI. However there may be a different type of construction on which the microvia material is added to a PWB core ([C]). The numbers refer to the number of HDI layers applied to either side of the core.

For instance, an HDI PWB with two layers of HDI on one side of the core and one layer of HDI on the other side of the core would be:

2[C]1

Thus, the following definitions apply to all forms of HDI:

TYPE I 1 [C] 0 or 1 [C] 1 – with through vias from surface to surface.

TYPE II 1 [C] 0 or 1 [C] 1 – with buried vias in the core and may have vias from surface to surface.

TYPE III ≥ 2 [C] ≥ 0 – with through vias buried in the core and may have vias from surface to surface.

TYPE IV ≥ 1 P ≥ 0 – where P is a passive substrate with no electrical connection.

TYPE V Coreless constructions using layer pairs.

TYPE VI Alternate constructions.

7.1.1 HDI Type I Constructions – 1[C]0 or 1[C]1 This construction describes an HDI in which there are both microvias and conductive vias used for interconnection. Type I constructions describe the fabrication of a single microvia layer on either one (1[C]0) or both (1[C]1) sides of an PWB substrate core.

The PWB substrate core is typically manufactured using conventional PWB techniques and may be rigid or flexible. The substrate can have as few as one circuit layer or may be as complex as any number of innerlayers.

The example in Figure 7-1 shows a 1[C]1 Type 1 construction. In this construction a single layer of dielectric material is placed on both sides of the core substrate. Microvias are formed connecting layer 1 to layer 2 and layer n to layer n-1. A hole is then formed connecting layer 1 to layer n. The microvias and holes are then metallized (they can be filled with conductive material if required), layer 1 and layer n are circuitized, and fabrication is completed.

Table 7-1 includes typical feature sizes for these constructions.

7.1.2 HDI Type II Constructions – 1[C]0 or 1[C]1 Type II constructions have the same number of HDI layers as Type I. The core can also be single-sided, double-sided, or multilayer as in Type I. The main difference is the core construction. In a Type II, the through holes only connect the outer and any inner layers of the core.

The example in Figure 7-2 shows a 1[C]1 Type II construction, which has two through vias in the core substrate formed prior to applying the HDI dielectric layers. Both vias connect layer 2 to layer n-1. The via on the right is

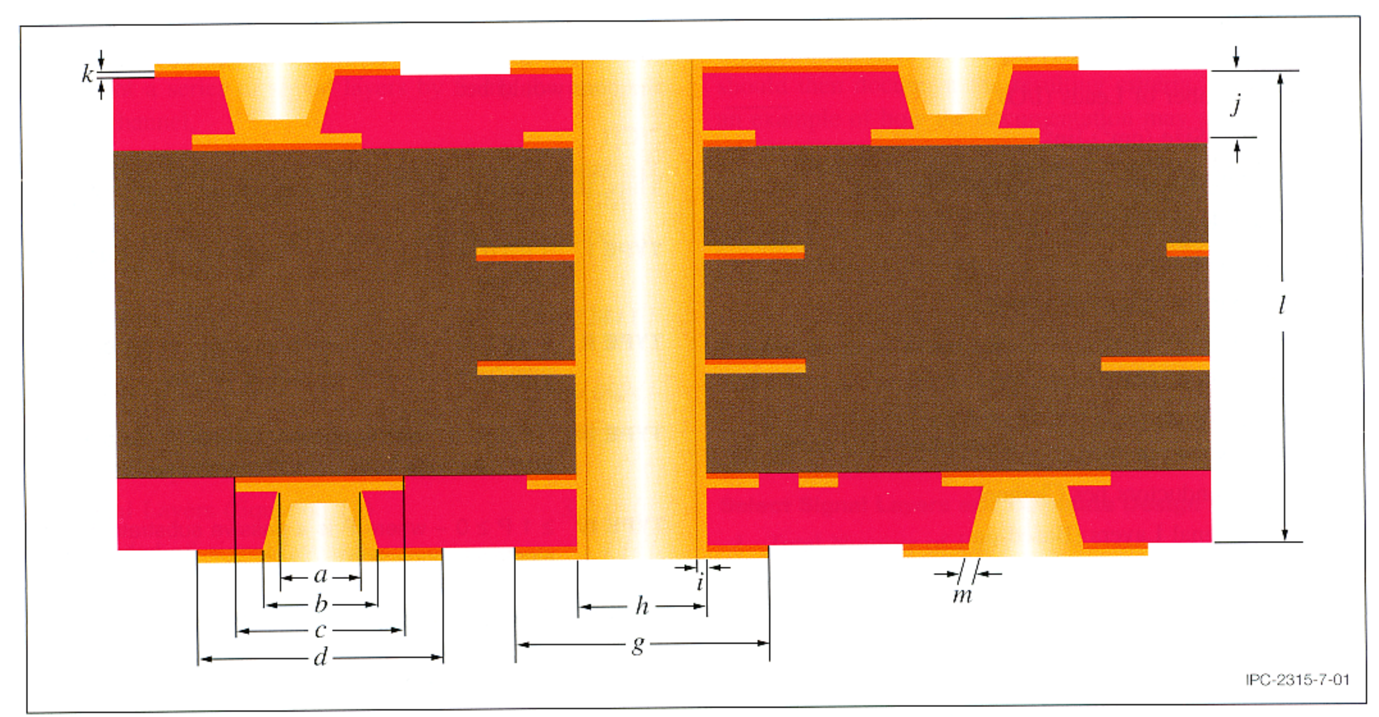


Figure 7-1 Type I HDI Construction

filled with a conductive paste. The via on the left is filled with HDI dielectric.

Microvias on layer 1 and layer n make the connection to the conductors on layer 2 and layer n-1, making the connection with the core vias. If needed, Type II constructions can also have vias formed connecting layer 1 directly to layer n (this is displayed in Figure 7-2).

Table 7-1 includes typical feature sizes for these constructions.

7.1.3 HDI Type III Constructions – ≥2[C]≥0 Type III constructions describe an HDI in which there are plated microvias, paste-filled holes, and PTHs used for interconnection. Type III constructions are distinguished by having at least two microvia layers on at least one side of a substrate core. The substrate core is usually manufactured using conventional PWB techniques, may be rigid or flexible, and can have as few as one or as many as any number of layers with buried vias.

The example in Figure 7-3 shows a substrate core that has been applied with a dielectric layer on each side. Microvias have been formed connecting layer 2 to layer 3 and layer n to layer n-1. The top layer is then metallized, a second dielectric layer is applied to it, and microvias are formed connecting layer 1 to layer 2. A PTH is then formed, connecting layer 1 to layer n, and the microvias and PTH are then metallized or filled with a conductive material. Layer 1 and layer n are then circuitized and fabrication is completed.

Table 7-1 includes typical feature sizes for these constructions.

7.1.3.1 Type III HDI with Stacked Microvias Figure 7-4 displays an example of a Type III HDI board with stacked microvias.

7.1.3.2 Very Complex TYPE III HDI Figure 7-5 displays a very complex HDI board, which utilizes staggered vias, a PTH, microvias filled with conductive paste, and several HDI layers.

Table 7-1 gives typical feature sizes for these constructions.

7.1.4 HDI Type IV Constructions – >[P]0 Type IV constructions describe an HDI in which the microvia layers are used as RDLs over an existing predrilled passive substrate. Additional RDLs can be added sequentially. The core substrate is usually manufactured using conventional PWB techniques and may be rigid or flexible. The function of the core is passive, yet it may be used for thermal or CTE management (the core doesn't perform an electrical function.).

The example in Figure 7-6 shows a passive substrate core that has been applied with a dielectric layer on each side. That layer is then plated and a second layer is applied to each side. Microvias are then formed connecting layer 1 to layer 2 and layer n to layer n-1. A via is then formed, which passes between a preformed opening in the core, connecting layer 1 to layer n.

Table 7-1 includes typical feature sizes for these constructions.

7.1.5 Type V Constructions (Coreless) – Using Layer Pairs Type V constructions describe an HDI in which

Table 7-1 Typical Feature Sizes for HDI Constructions

Symbol	Feature	Preferred Producibility Range (µm) [mil]	Reduced Producibility Range (um) [mil]
a	Microvia diameter at target land (as formed, no plating)	100 - 150 [3.937 - 5.906]	<100 [3.937]
b	Microvia diameter at capture land (as formed, no plating)	125 - 200 [4.921 - 7.874]	100 [3.937] min., 250 [9.843] max.
c	Microvia target land size = [(a + 2x annular ring) + FA [(1)]		
	FA for c =	150 - 250 [5.906 - 9.843]	<150 [5.906]
d	Microvia capture land size = [(b + 2x annular ring) + FA [(1)]]		
	FA for d =	150 - 250 [5.906 - 9.843]	<150 [5.906]
e	External conductor trace width	100 - 200 [3.937 - 7.874]	<100 [3.937]
f	External conductor spacing	100 - 200 [3.937 - 7.874]	<125 [4.921]
g	Through via land size = [(h + 2x annular ring) + FA [(1)]]		
	FA for g =	250 - 300 [9.843 - 11.81]	<250 [9.843]
h	Through via diameter (as formed, no plating)	250 - 350 [9.843 - 13.78]	<250 [9.843]
i	Minimum through via hole wall plating thickness	16 - 20 [0.630 - 0.787]	>20 [0.787]
j	Dielectric thickness (HDI blind microvia layer) [(2)]	35 - 100 [1.38 - 3.937]	<35 [1.38] or >100 [3.937]
k	External Cu foil thickness (if Cu foil utilized)	9 - 18 [0.35 - 0.709]	<9 [0.35]
l	Board thickness (excluding external conductors)	400 - 800 [15.748 - 31.50]	<450 [17.72]
m	Minimum blind microvia hole plating thickness	10 - 18 [0.394 - 0.709]	>18 [0.709]
n	Minimum buried via hole wall plating thickness [(3)]	11-13 [0.433 - 0.512]	>17 [0.669]
o	Buried via diameter (as formed, no plating)	200 - 300 [7.874 - 11.81]	<200 [7.874]
p	Buried via land size = [(o + 2X annular ring) + FA [(1)]]		
	FA for p =	250 - 300 [9.843 - 11.81]	<250 [9.843]
q	Buried via core thickness (excluding outermost conductors)	125 - 750 [4.921 - 29.528]	<125 [4.921]
r	Buried via Cu foil thickness (outermost layer)	9 - 18 [0.35 - 0.709]	<9 [0.35]
s	Internal conductor trace width	75 - 150 [2.95 - 5.906]	<75 [2.95]
t	Internal conductor spacing	100 - 150 [3.937 - 5.906]	<100 [3.937]
u	Core thickness (excluding conductors)	100 - 200 [3.937 - 7.874]	<100 [3.937]
(p+c)/2	Staggered via pitch	200 - 275 [7.874 - 10.83]	<200 [7.874]
ASPECT RATIOS			
(k + j) / a	Microvia plating aspect ratio	0.5:1 - 0.7:1	>0.7:1
(2k + l) / h	Thru via hole aspect ratio	4:1 - 8:1	>8:1
(2r + q) / o	Buried via aspect ratio	4:1 - 8:1	>8:1

(1) FA = Fabrication Allowance as defined in IPC-2221
(2) Measured from top surface of Layer 2 Cu to bottom surface of Layer 1 Cu
(3) Dielectric core thickness <750 µm [29.52 mil] For greater core thickness refer to current revision of IPC-6012.

there are both plated microvias and conductive paste interconnections through a co-lamination process. There is essentially no core to this type of construction since all layer pairs have the same characteristics. Type V constructions consist of the fabrication of an even number of layers that are laminated together at the same time the interconnections are made between the odd and even layers. This type of construction is neither build-up nor sequential; it is a single lamination process.

The layer-pair substrates are prepared using conventional processes (i.e., etching, plating, and buried vias), and the substrates may be rigid or flexible. The layer pairs are joined together using B-Stage resin systems or some other form of dielectric adhesive into which conductive adhesive has been placed. This joining material is used to make the appropriate interconnections. External layers may consist of a single conductive layer, provided its companion layer pair is on the opposite side.

Figure 7-7 gives an example of a coreless construction using three layer pairs that have been connected in lamination with patterned conductive material and a dielectric adhesive.

Table 7-1 includes typical feature sizes for these constructions.

7.1.6 Type VI Constructions Type VI constructions describe an HDI in which the electrical interconnection and mechanical structure are formed simultaneously. The layers

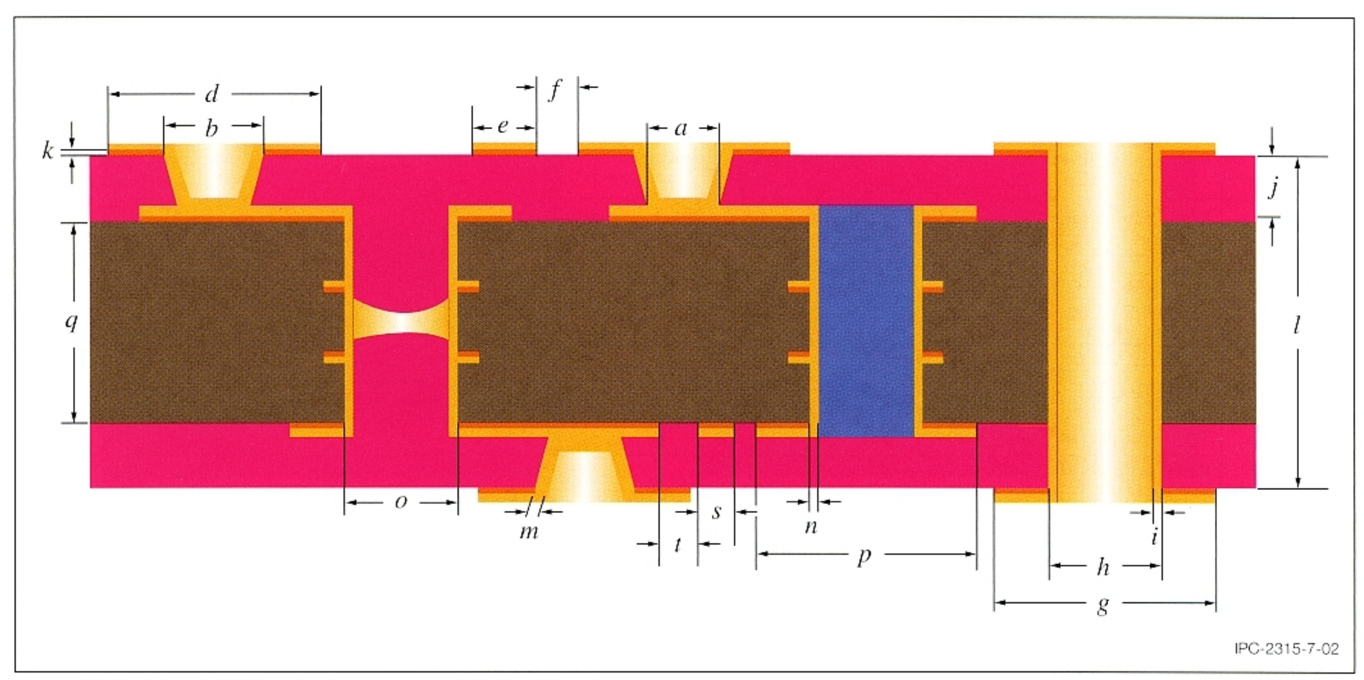


Figure 7-2 Type II HDI Construction

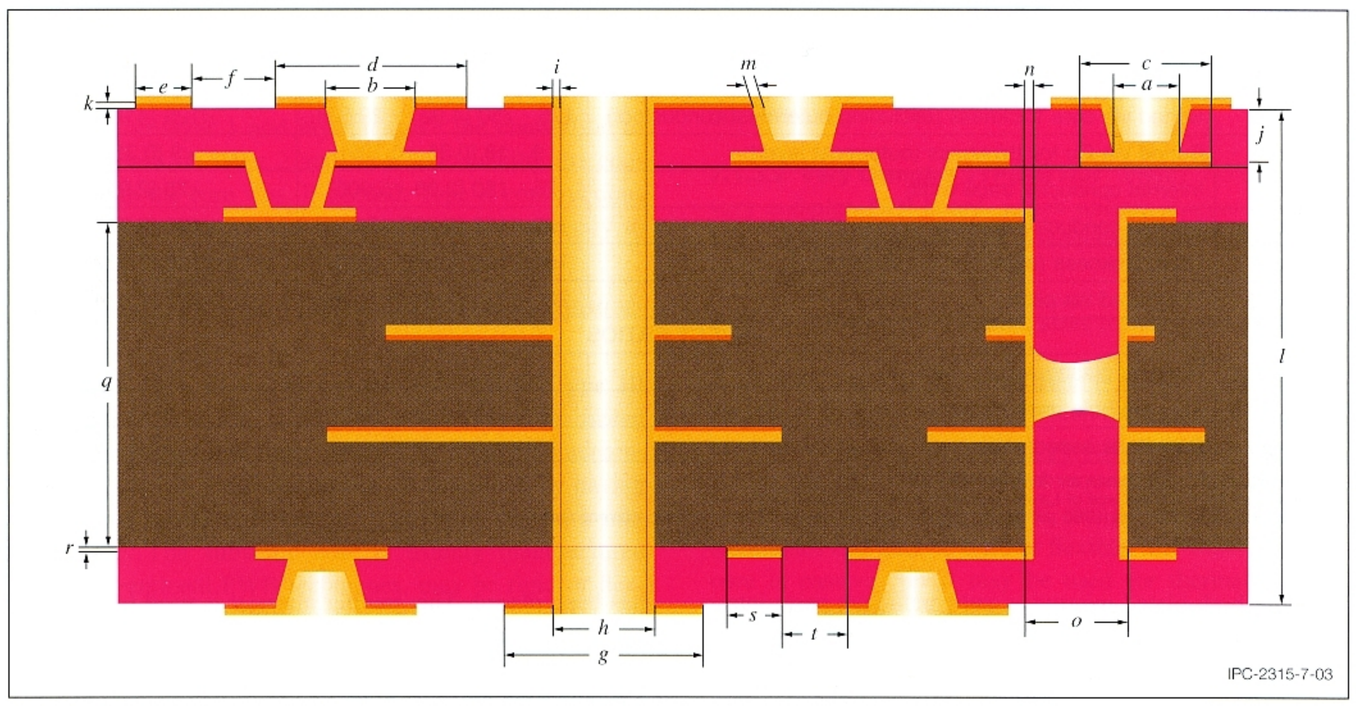


Figure 7-3 Type III HDI Construction

may be formed sequentially or co-laminated, and the conductive interconnection may be formed by means other than electroplating (i.e., anisotropic films/pastes, conductive paste, dielectric piercing posts, etc.).

Figure 7-8 gives an example of a Type VI construction that was manufactured using piercing posts. The posts, which are made up of a conductive element, are attached to an unreinforced layer of copper, and the bonding process and interconnections are made by adding prepreg and laminating the PWB together in one step.

Table 7-1 includes typical feature sizes for these constructions.

7.2 Producibility The designer should not specify the type of manufacturing methods used to prepare the microvia, but should indicate to the fabricator the size of

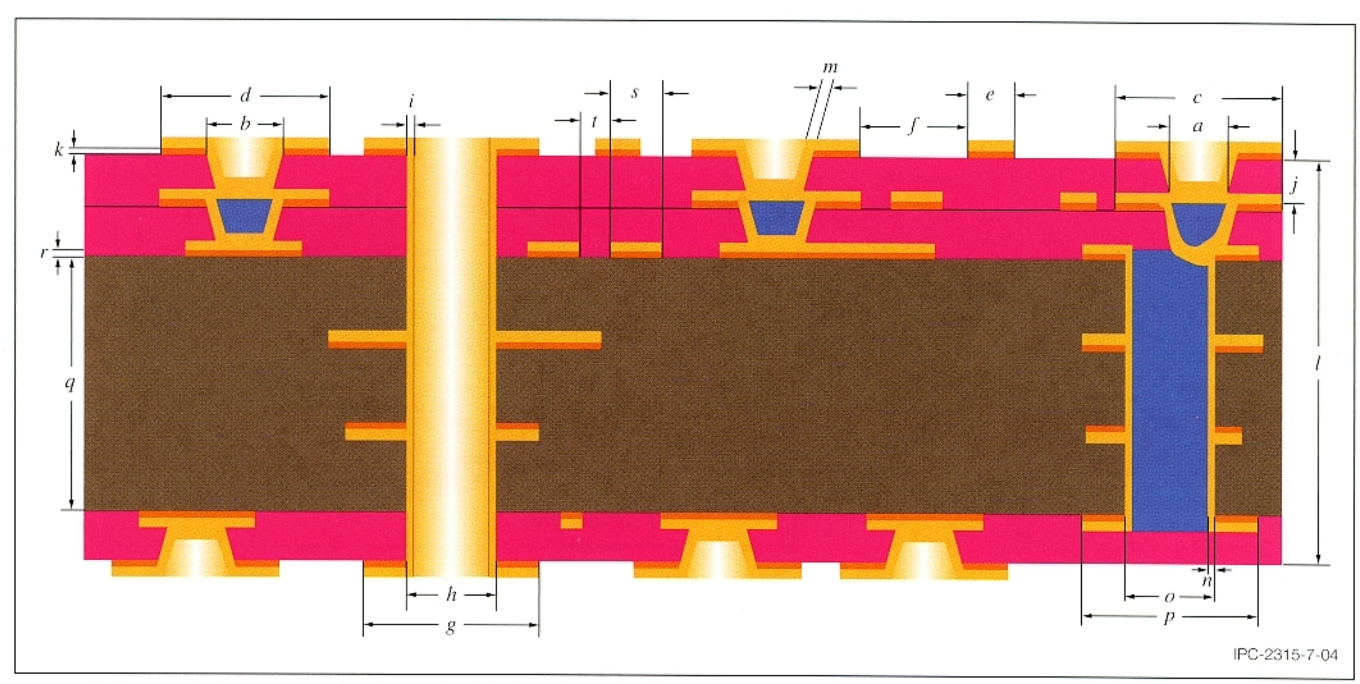


Figure 7-4 Design Example for Type III HDI with Stacked Microvias

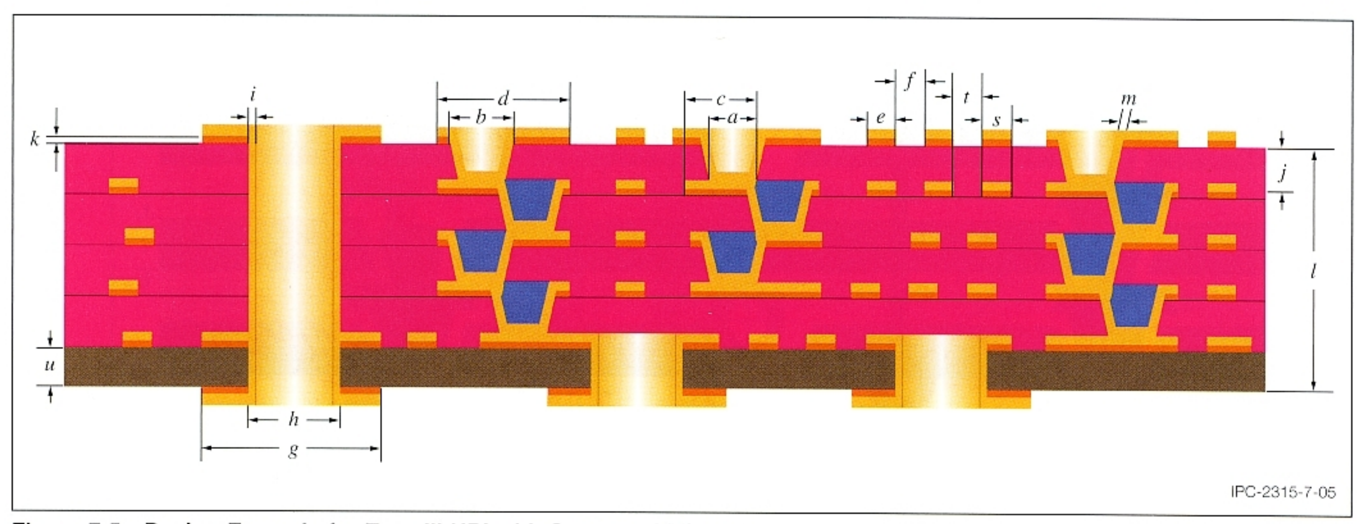


Figure 7-5 Design Example for Type III HDI with Staggered Microvias

the capture land in the design. The designer should be aware that not all fabricators have equal capabilities in the areas of fine pitch imaging, etching, layer-to-layer alignment, via formation, and plating.

Table 7-1 provides ranges for dimensions of the features found in PWBs that utilize microvia structures. The ranges for each feature were set considering the present capabilities of manufacturers that currently produce microvias. The designer should be aware that more aggressive design rules will significantly impact the producibility and cost of a PWB.

Circuits designed within the standard producibility ranges will be more readily produced, have relatively higher yields, and therefore can be fabricated at lower cost. Selection of more stringent design rules may limit the number of manufacturers capable of producing such a board. Therefore the design rules most appropriate for the application should be selected.

7.3 General Design Rules for Other HDI Constructions

This section is intended to provide design rules common to all known HDI constructions and materials. The general design rules are assumed to be the lowest cost and easiest to fabricate.

7.3.1 Staggered Via Figure 7-2, Figure 7-3, and Figure 7-9 display examples of staggered vias, which can be used with Table 7-1 to determine its specific design rules.

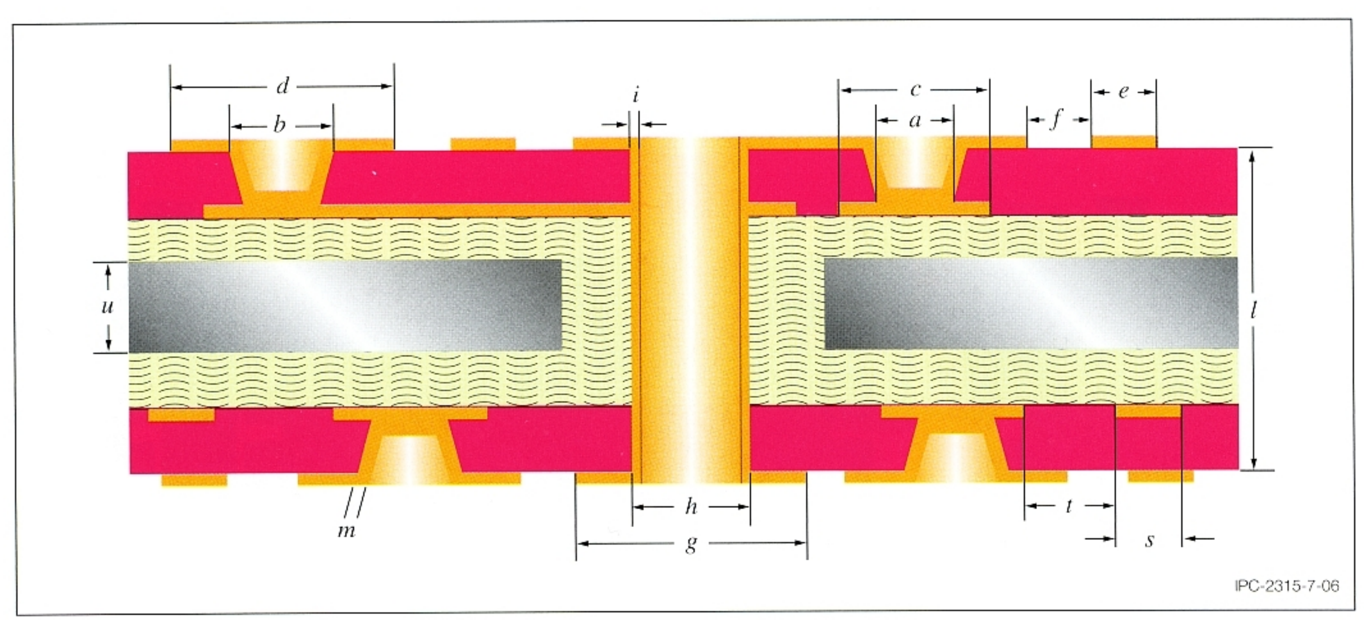


Figure 7-6 Type IV HDI Construction

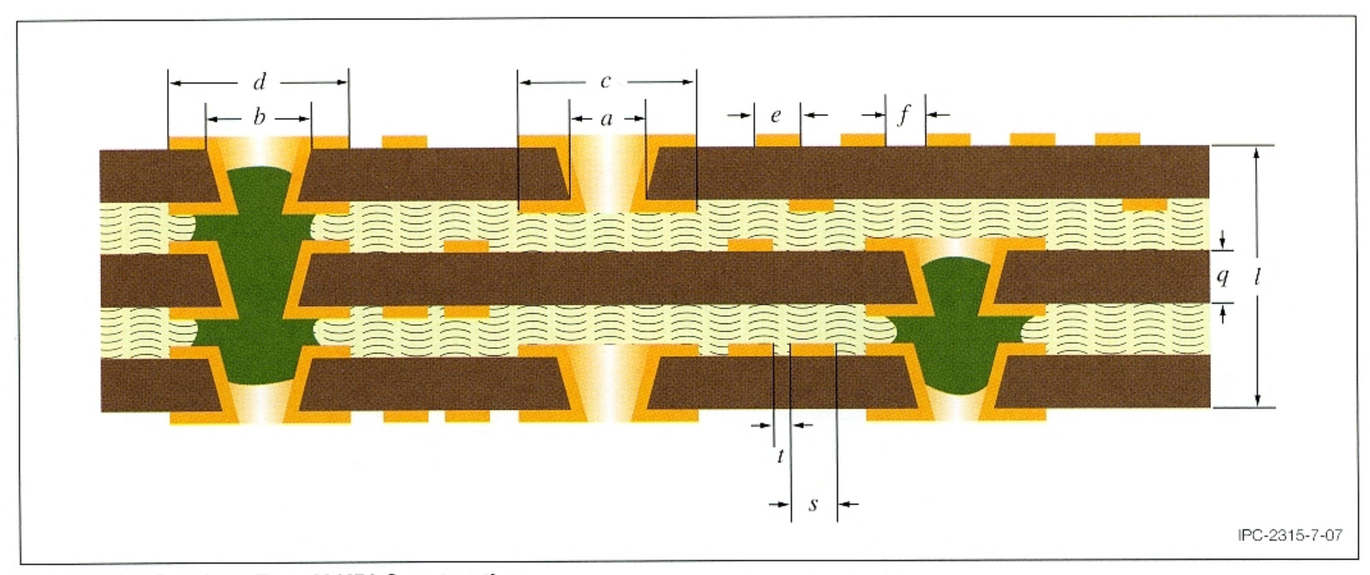


Figure 7-7 Coreless Type V HDI Construction

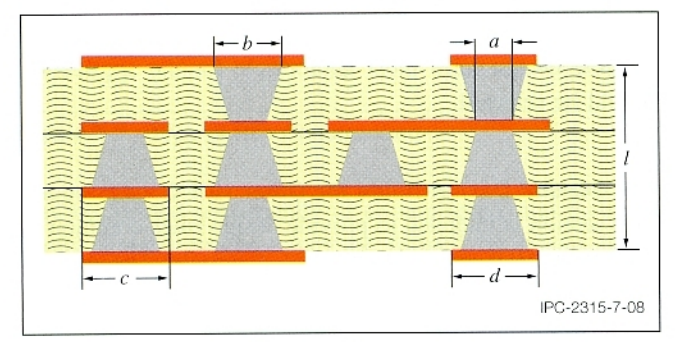


Figure 7-8 Type VI Construction

7.3.2 Via-In-Land Figure 7-10 displays some common via-in-land design elements that should be taken into consideration for HDI boards.

7.4 Alternative Construction HDI Design Rules This section covers design rules specific to unique methods of fabrication that are not generic to all methods of HDI fabrication. Variable depth microvias have a number of possible design variations (see 7.4.1).

7.4.1 Variable Depth Microvias Figure 7-11 displays an example of an HDI board utilizing a variable depth microvia.

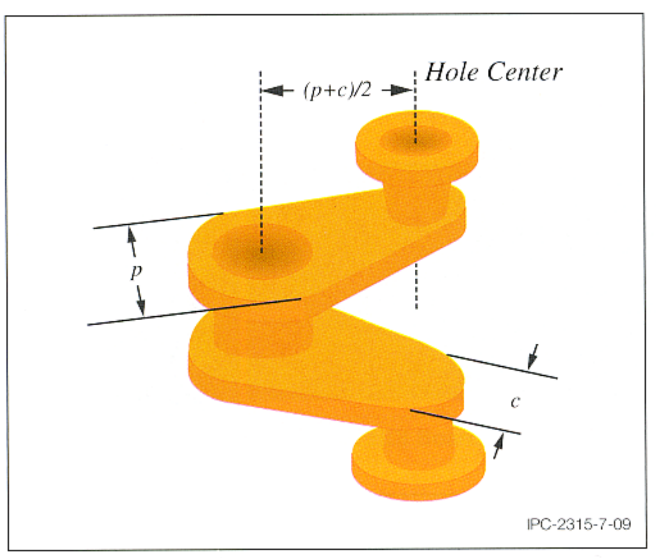


Figure 7-9 Staggered Vias

7.4.2 Staggered Microvias Figure 7-2, Figure 7-3, Figure 7-5, and Figure 7-12 display examples of HDI boards with staggered microvias.

7.4.3 Co-Lamination with Conductive Paste Figure 7-13 displays an example of an HDI board that has been colaminated with conductive paste. Table 7-2 gives the design requirements for these HDI boards.

7.4.4 Conductive Ink Sequential Buildup Figure 7-14 displays an example of an HDI board that has been built up using conductive ink.

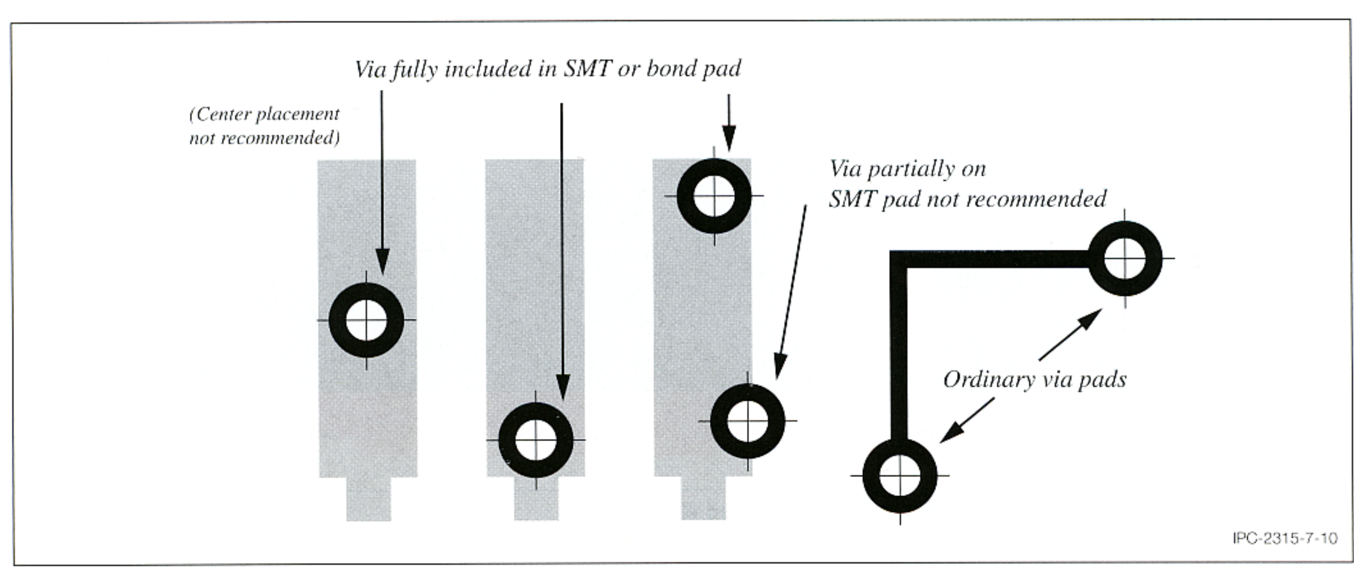


Figure 7-10 Via-In-Land Design Example

Table 7-2 Conductive Paste Co-Lamination Design Rules

Symbol	Feature	Preferred Producibility Range (µm) [mil]	Reduced Producibility Range (µm) [mil]
v	Conductive paste spread	200-250 [7.874-9.843]	<200 [7.874]
w	Conductive paste spacing	≥250 [9.843]	<250 [9.843]

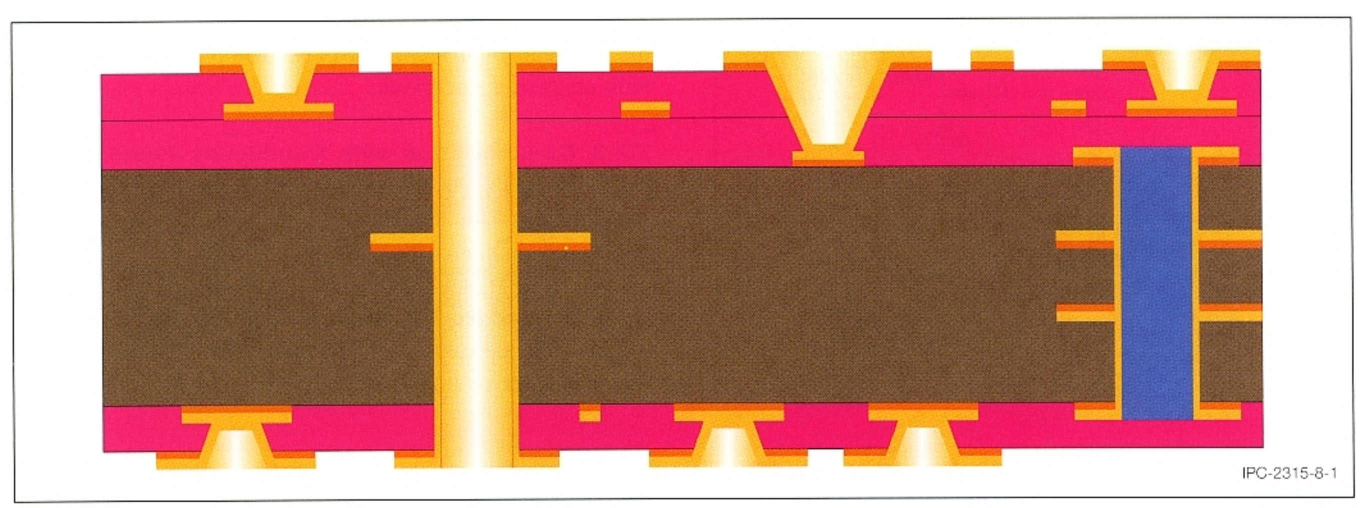


Figure 7-11 Design Example for HDI Board with Variable Depth Microvias

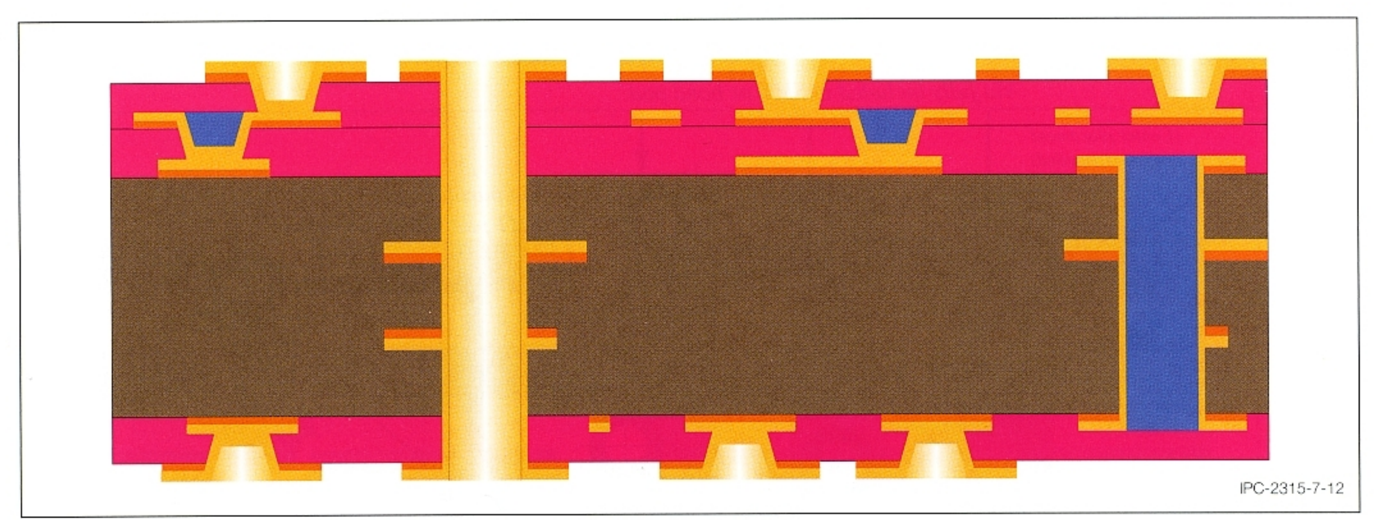


Figure 7-12 Design Example for HDI Board wtih Staggered Microvias

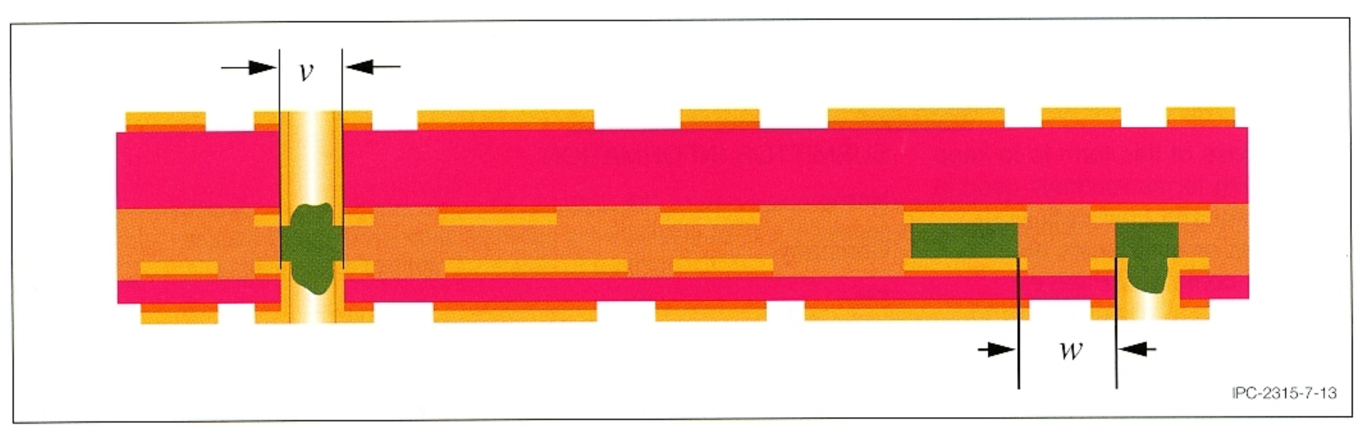


Figure 7-13 Design Example for HDI Board Co-Laminated with Conductive Paste

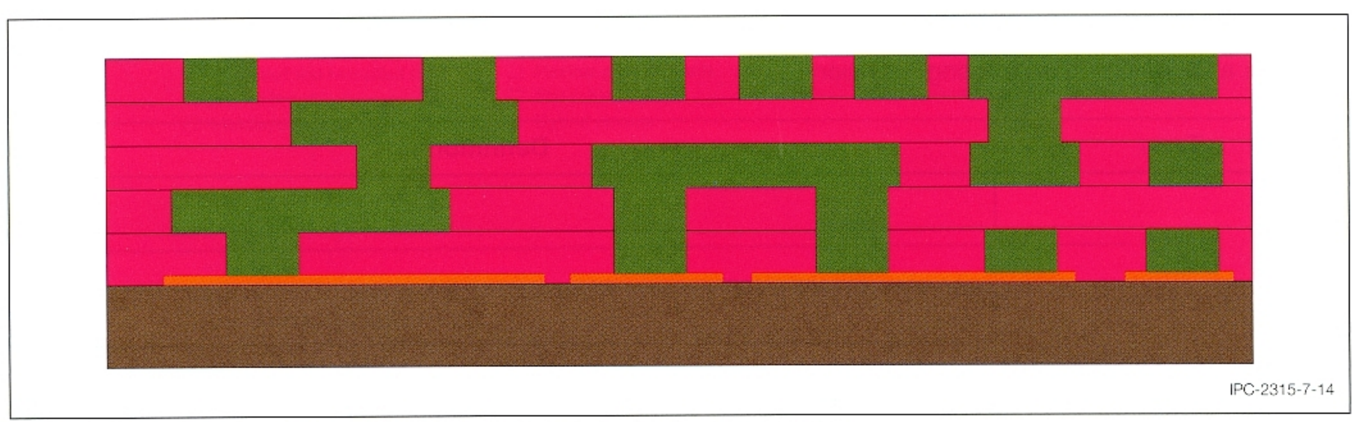


Figure 7-14 Design Example for HDI Board Utilizing Conductive Ink Build Up



ANSI/IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits Definition Submission/Approval Sheet

The purpose of this form is to keep current with terms routinely used in the industry and their definitions. Individuals or companies are invited to comment. Please complete this form and return to:

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Committee 2-30

Date of Initial Review: ______________________
Comment Resolution: ______________________
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Our facility manufactures and sells to other companies, printed wiring boards or other electronic interconnection products on the merchant market.

WHAT PRODUCTS DO YOU MAKE FOR SALE?

- ☐ One-sided and two-sided rigid printed boards
- ☐ Multilayer printed boards
- ☐ Flexible printed boards
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- ☐ SMT
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- ☐ Mixed Technology
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Name of Chief Executive Officer/President______________________

■ **OEM – MANUFACTURERS OF ANY END PRODUCT USING PCB/PCAS OR CAPTIVE MANUFACTURERS OF PCBS/PCAS**

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IS YOUR INTEREST IN:

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____

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